Final Lab Report: Full Adder

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Group 5

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Abstract:

After a full quarter in 120A of practicing the techniques involved in making steady state semiconductor devices including applying photoresist, optical lithography, growing oxides, mask alignment, and familiarizing ourselves with the equipment and tools necessary to perform each part of the process, we were given the task of designing and fabrication our own circuit designs.

The first week or two of this class was spent designing our circuits on L-Edit, which we sent in to be made into masks. We decided to be little ambitious and design a full adder, as our group was very familiar with how it was supposed to perform, the gates and connections involved, and it seemed fairly easy to test once the circuit was made. We did some research on how we could make a full adder out of XOR, AND, and OR gates, and then more research on how to design these individual gates using only NMOS transistors. After verifying that our design would function properly, we got to laying it out on the L-Edit software. This was a new experience for all of us, but after overcoming the slight learning curve, it became fairly easy to navigate and we were able to come up with a design that we all agreed was good.

Once the masks arrived, we employed the skills that we learned last quarter in 120A to make chips with our own design. The fabrication process was fairly smooth, as we had the skills necessary from last quarter and knew what mistakes to avoid. We credit our success this quarter to following every step exactly, knowing which step to pick up on when it was a new day, doing every calculation multiple times, being meticulous about recording data, observations, and measurements, and taking pictures as often as possible. These are things that we failed to do last quarter that we ended up regretting.

Once our chips were fabricated, we tested them to see if we were getting the expected outputs from each of our gates and the full adder. During this testing phase is when we realized a lot of the problems with our circuit design, and things we could have done differently. Luckily, we were getting the correct outputs in terms of high and low signals, but having a diode as a load made analysis quite difficult and we didn't really have solid expected values to compare our actual values with. The lack of variance in our features also made it difficult to analyze and compare our data.

Overall, this lab was an extremely educational experience. We were able to learn from our mistakes last quarter and made new mistakes that we also learned from. The skills that we acquired over the course of this quarter, including circuit design, fabrication, and testing techniques, are both applicable and important as semiconductor fabrication is a rapidly advancing area of study in electrical engineering.

Final Device Under Microscope

Figure 1

Design

Our design started with a single MOSFET. We choose a 50 by 20µm design because it was compact and performed well last quarter (figure 2). We made large (100 by 100µm) testing pads for all of our devices.

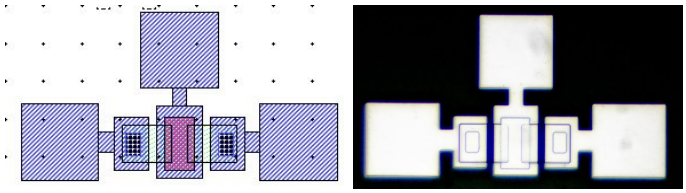


Figure 2: MOSFET design and and image

Instead of loading our MOSFET with a resistor (which are often large and wasteful on a space-constrained design), we chose to use a diode as our loading element (figure 3). This was accomplished simply by connecting the metal layer between the gate and drain. We swapped the width and length of the gate to increase its length and, thus, increase the load without altering the dimensions.

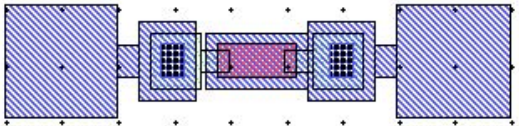


Figure 3: Diode design

Some of our gates required that we stack two transistors. This presented a problem, since we would need to double our load in order to accommodate two gates. To do this, we would have to increase the diode's gate length. We were concerned that simply doubling the diode length to 100µm might not give us twice the load, since diodes are non-linear. We resolved this issue by designing what we call our "double MOSFET". This device has two identical gates (also 50 by 20 µm) and has half the R_{ds} (figure 4). By keeping our gate sizes consistent throughout all our devices our hope was that we would reduce variability in our components and decrease the possibility of failure. It also made the design process easier, since we were easily able to swap components.

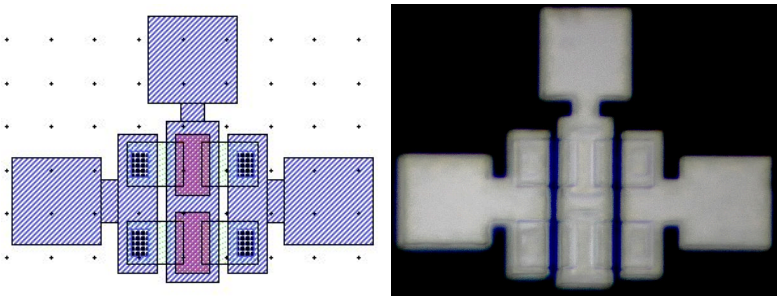


Figure 4: Double MOSFET design and image

The first gate we constructed was an OR gate, which we built by constructing a NOR followed by and inverter.

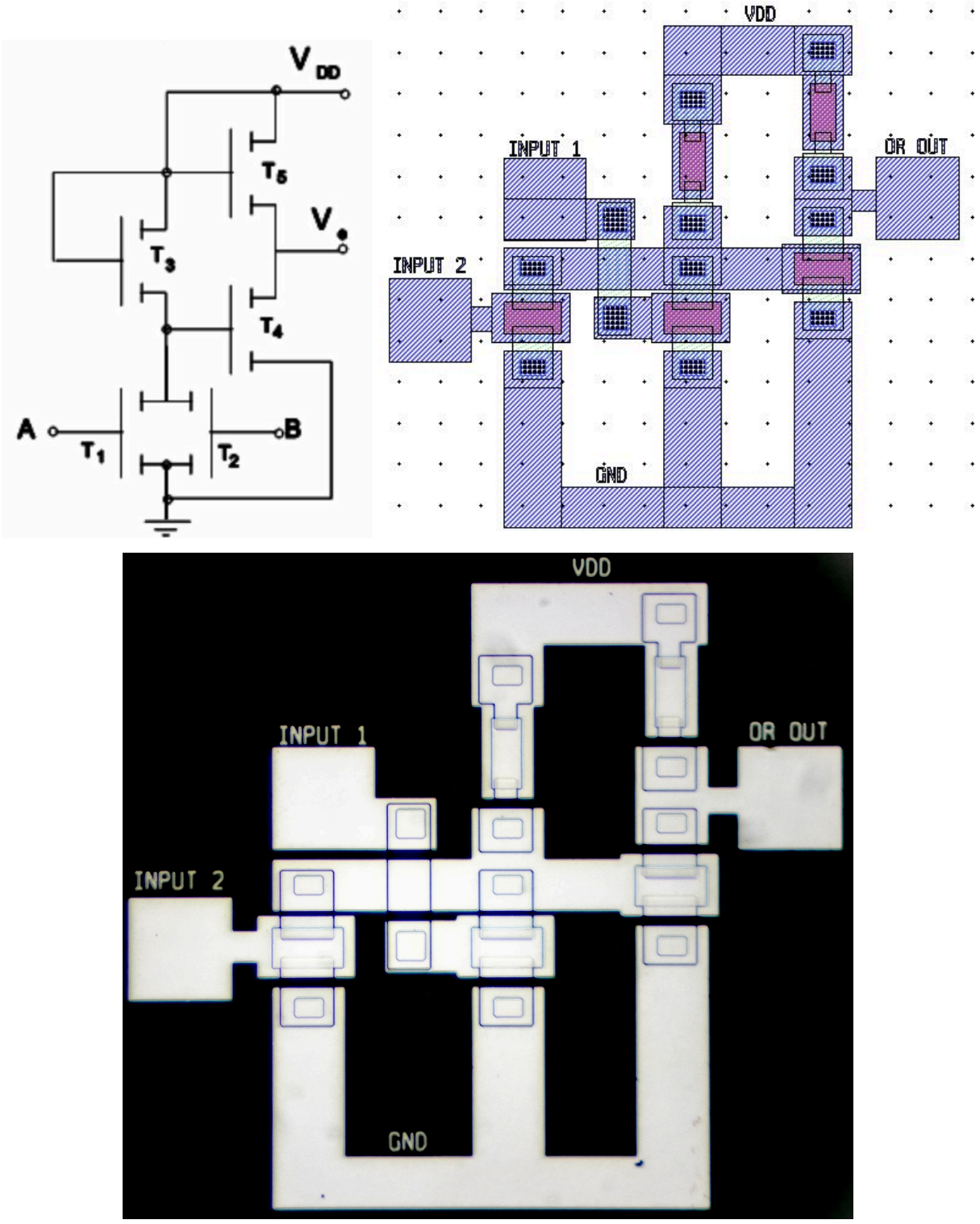
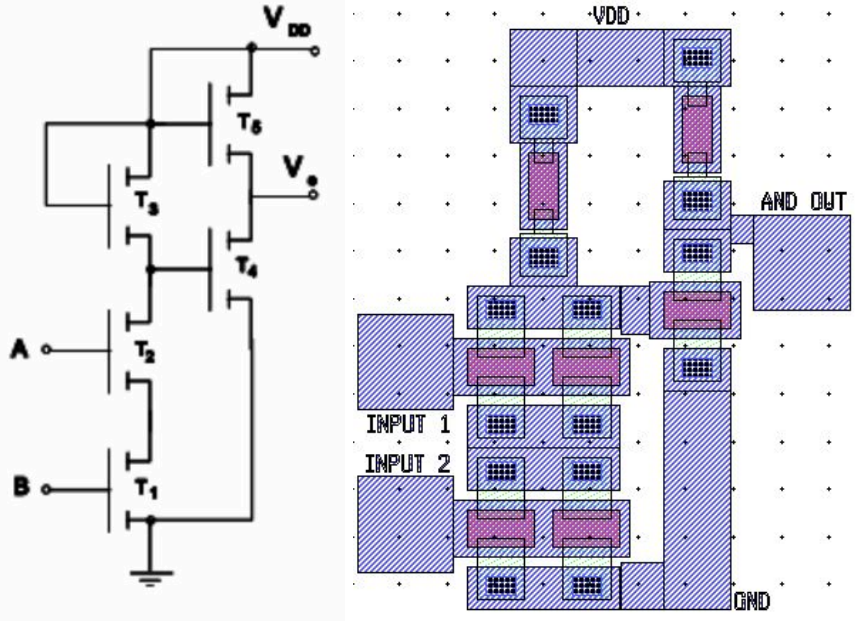


Figure 5: OR Gate schematic, design, and image

Next we designed an AND gate by placing an inverter after a NAND stage. The NAND gate required our double MOSFET.



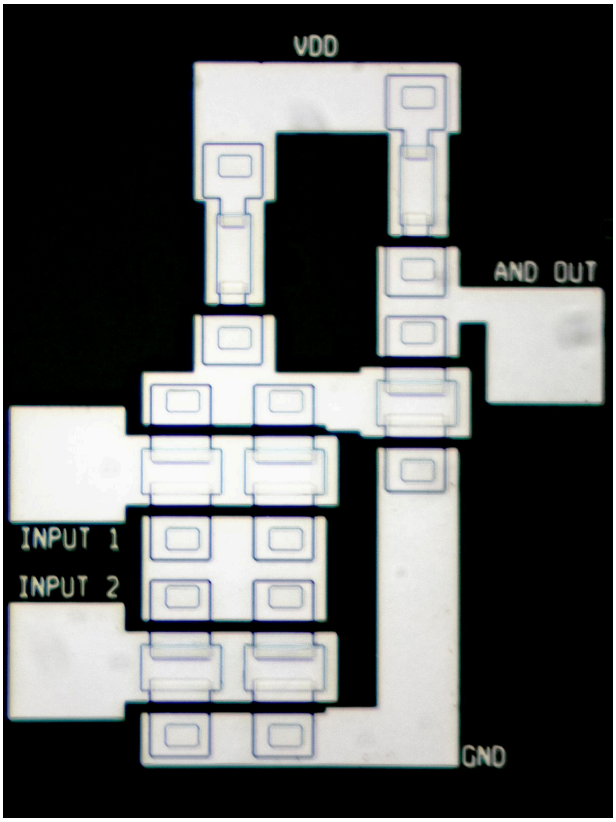


Figure 6: AND Gate

Our final and most complex gate was the XOR, which utilized both NAND and NOR gates.

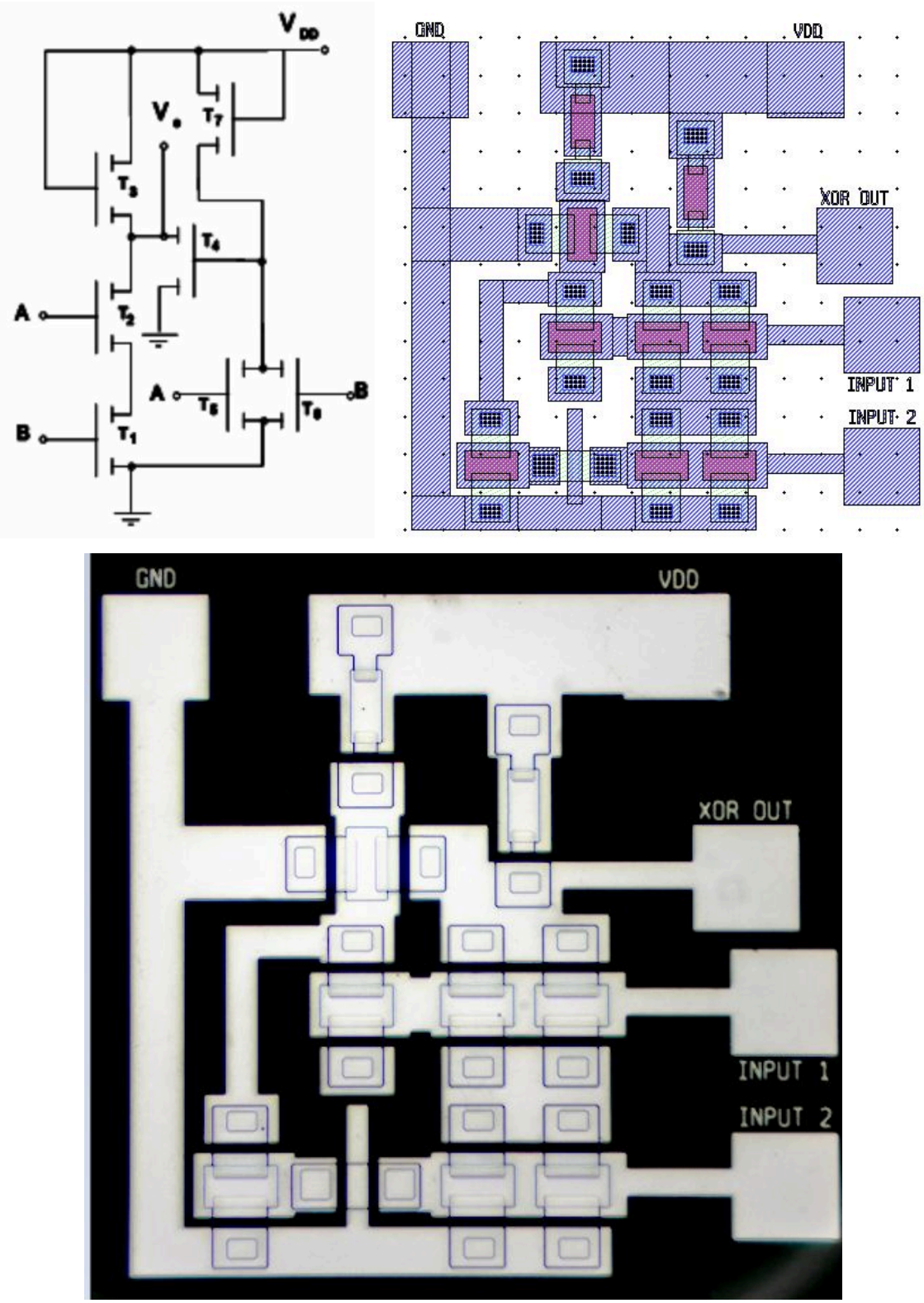


Figure 7: XOR Gate

In order to better understand the XOR gate, we performed some circuit simulations to verify the outputs.

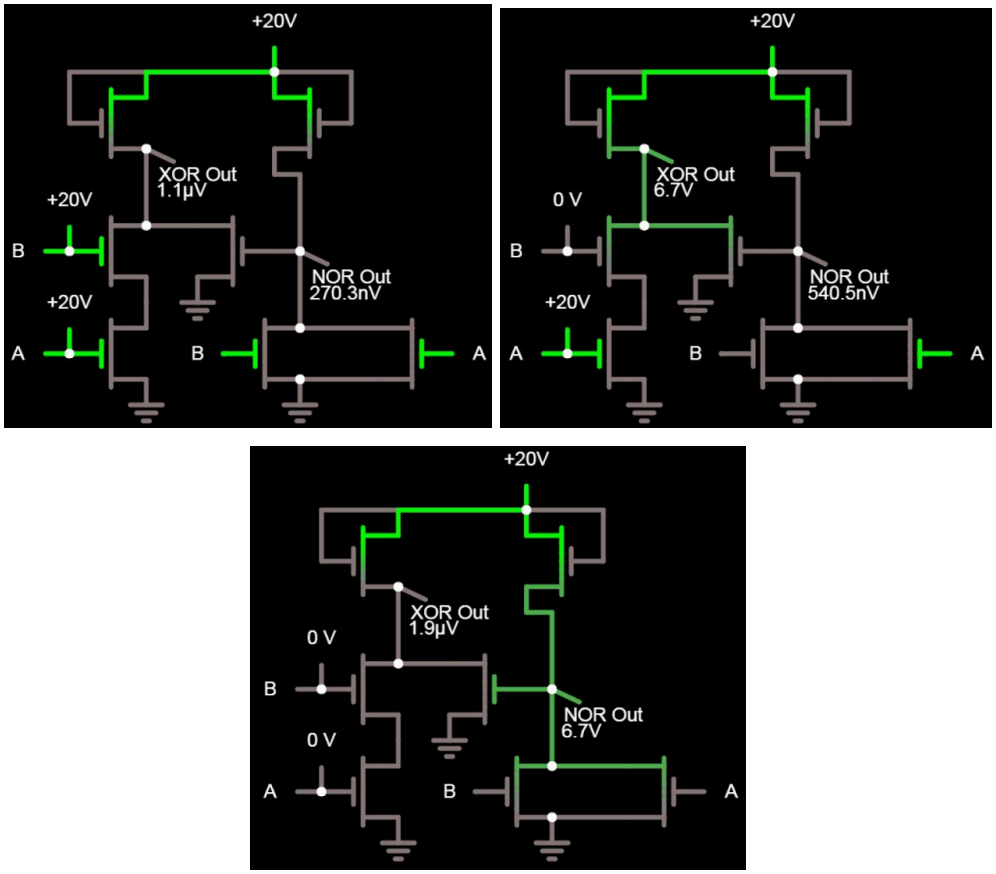


Figure 7: Diagrams from this Falstad simulation with various configurations of A and B input DC voltages

Our final design incorporated all three gates along with various symmetries and labels to facilitate the testing processes.

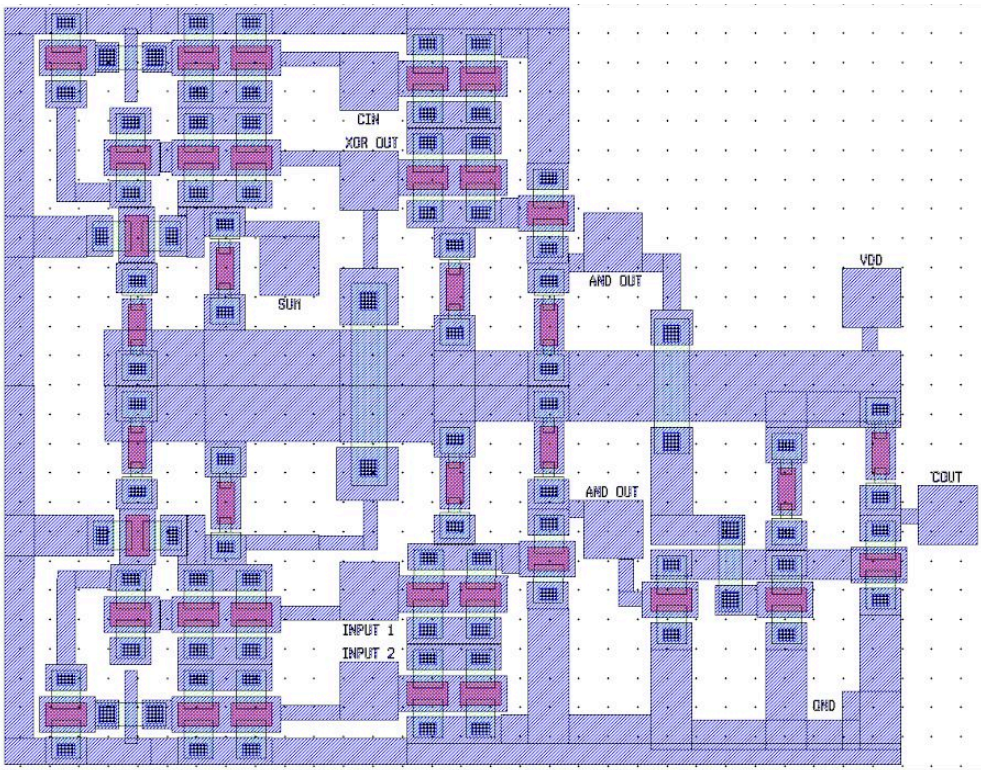


Figure 8: Full Adder design

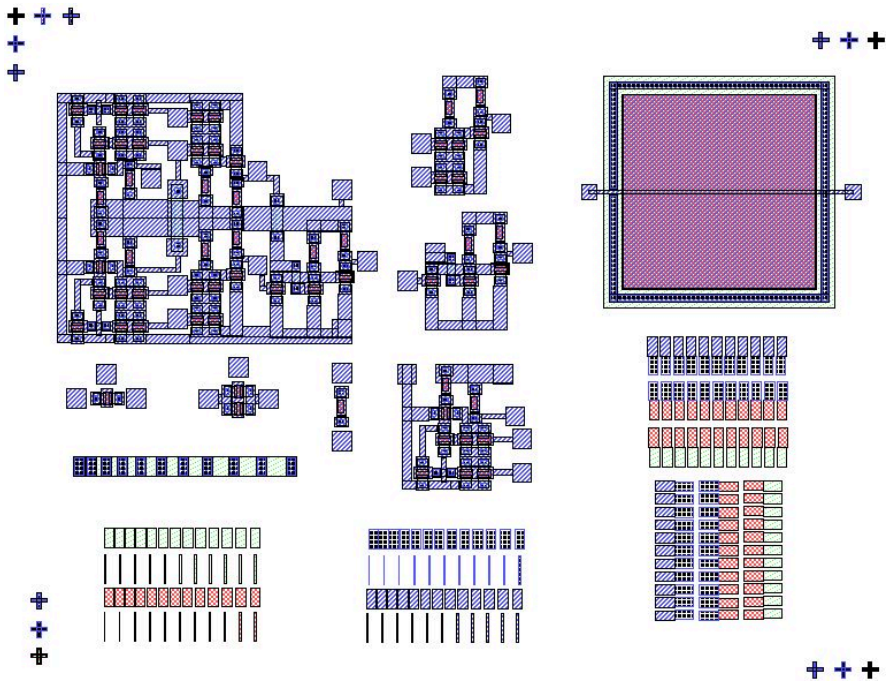


Figure 9: Complete Mask design

Our design also included other elements for aligning the masks, determining etch rate, and testing device performance.

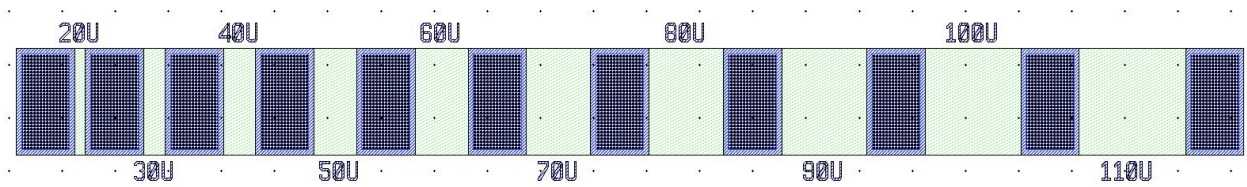


Figure 10: Transfer Length Measurement (TLM) Test Patern

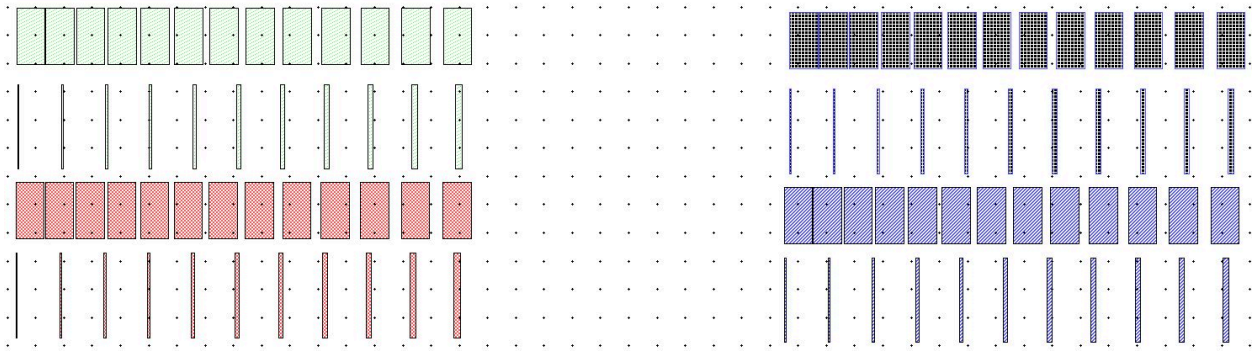


Figure 11: Etch Accuracy

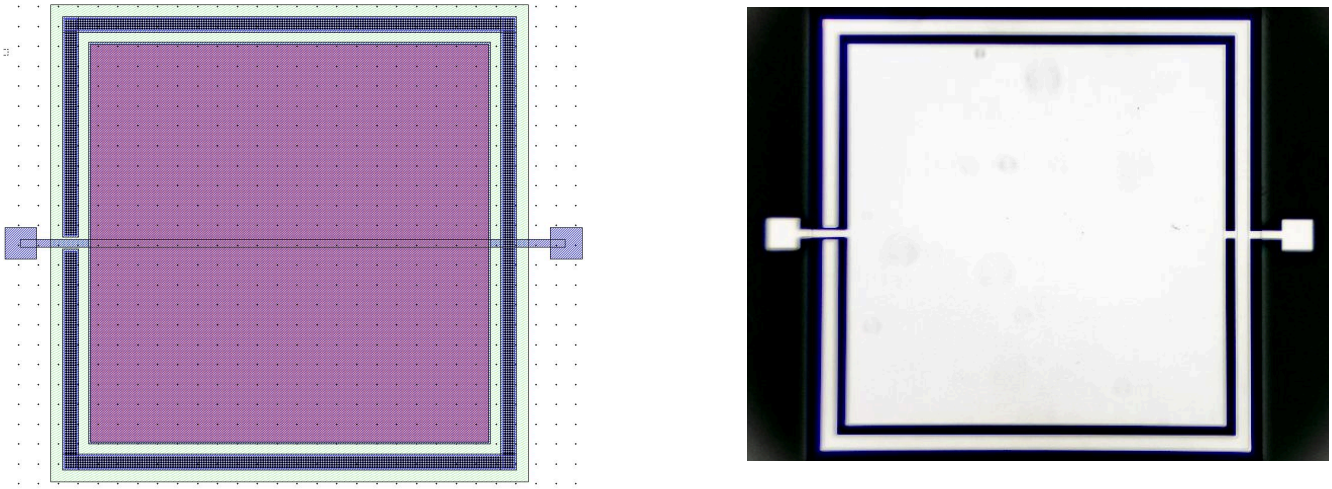


Figure 12: 1000x1000µm Capacitor

Procedure

Over the last two weeks we worked in the clean room in order to successfully fabricate a properly working MOSFET device. This involved multiple visits to the clean room where we worked with various processes, including oxidation, pre-deposition, drive-in, metal evaporation and lift-off along with multiple different wafer cleaning techniques to ensure the accuracy of a working device.

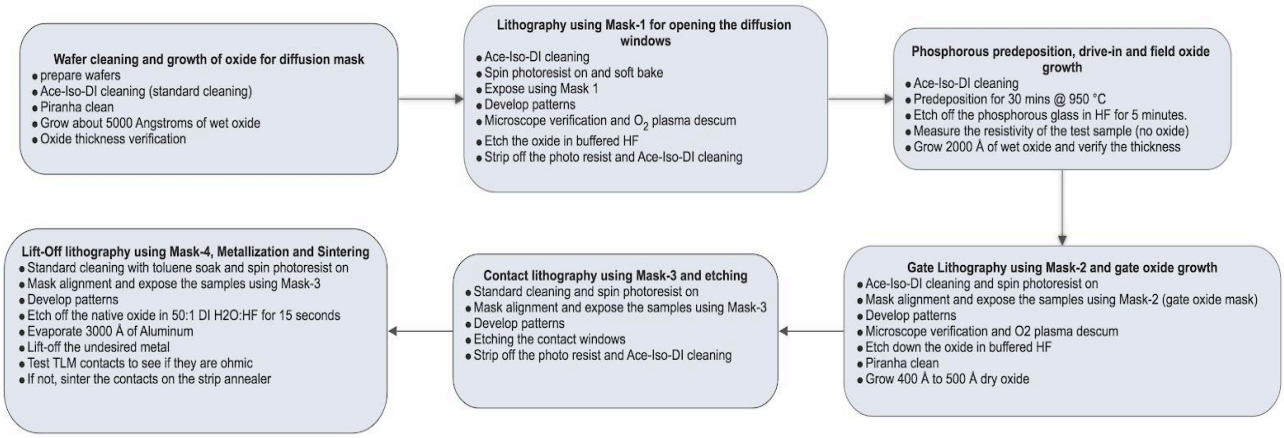


Figure 13: Flow Chart of Fabrication Process

Day 1: Wafer cleaning and growth of oxide for diffusion mask

After properly gowning up in clean room attire, we used the diamond tipped scribe to cleave two p-type <100> silicon wafers of 10-30 ohm-cm into 6 individual samples (Figure 1). We, then, cleaned each sample using proper wafer cleaning by immersing them in acetone (ACE) and isopropyl alcohol (ISO) before using the DI water and N_2 gas to dry them. Proceeding wafer clean, we measured the resistivity using the four point probe and got 16.35 ohm-cm, verifying the resistivity measurement that we wanted. Before oxidizing our wafers, we performed a piranha clean using a mixture of hydrogen peroxide (H_2O_2) and sulfuric acid (H_2SO_4) for ten minutes. We, then, cleaned our wafers with HF and DI water in order to remove any small layer of oxide that might have formed due to the peroxide. To operate the furnace, we followed several preparatory procedures, including preheating the furnace, setting the bubbler, and purging the system with N_2 gas. We then replaced the N_2 gas with O_2 gas. Placing our wafers into the furnace was a delicate procedure: first we put them on the sample holder, which was then placed in a boat (quartz elephant) that we pushed into the furnace with a glass rod. We began with a ten minute dry oxidation, followed by an 1 hr 10 minute wet oxidation (which we did by turning off the O_2 and turning on the process switch), and finishing with another ten minute dry oxidation. We took the wafers out of the furnace and after letting our wafers cool we measured the thickness of the SiO_2 layer with an Applied Materials ellipsometer and a Filmetrics thin film analyzer to get an initial layer thickness of around 5700 Å (Shown in images below). The

variations in the thicknesses is because of the temperature variation due to the placement of the chip in the furnace.

Sample	Thickness (Å)
A	5683
B	5604
C	5706
D	5668
E	5703
F	5784

Table 1: Initial Oxide Thickness on Samples

Day 2: Lithography using Mask-1 for opening the diffusion windows

After day 1, we had about 5600 Å of wet SiO_2 on our silicon bases. We started with standard Ace-Iso-DI cleaning, dehydration baking for 3 minutes, and placing wafers under the HMDS vapor deposition hood for 3 minutes. Then we spun photoresist on and soft baked for 1 minute. Then we used Mask-1 to expose diffusion regions and exposed under UV light for 12 seconds. We developed each chip at a time using 4:1 DI H_2O:AZ 400K developer for 75 seconds then examined them under the microscope.

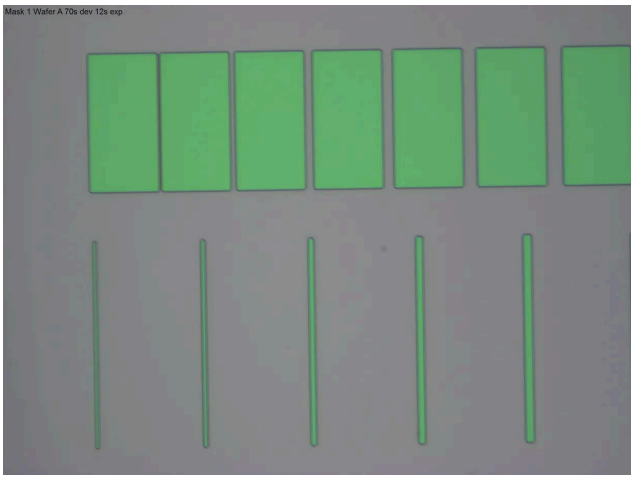


Figure 14: Mask 1 pattern with 75 seconds of development

Before we began our etching, we performed an O_2 plasma descum, which we did before every etching. Then we etched one chip to verify the etching rate and calculate how long does it take to etch off all 5600 Å oxide with 20% over-etching. Before etching, we immersed the wafer in DI for 1 minute with agitation before placing it in the HF. This prevents bubble formation and ensures uniform etching.

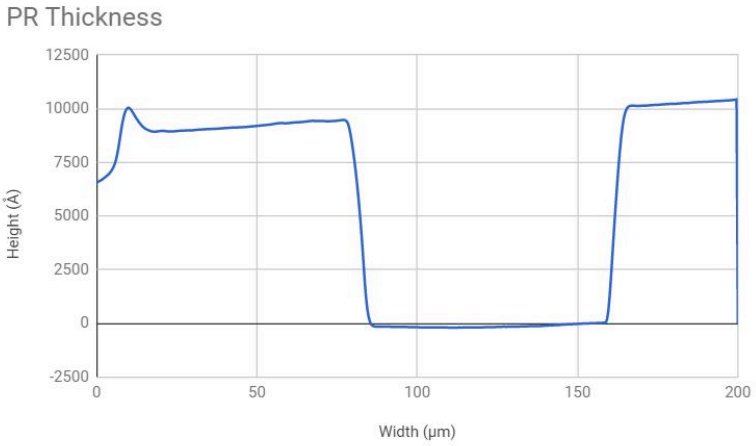


Figure 15: Photoresist thickness

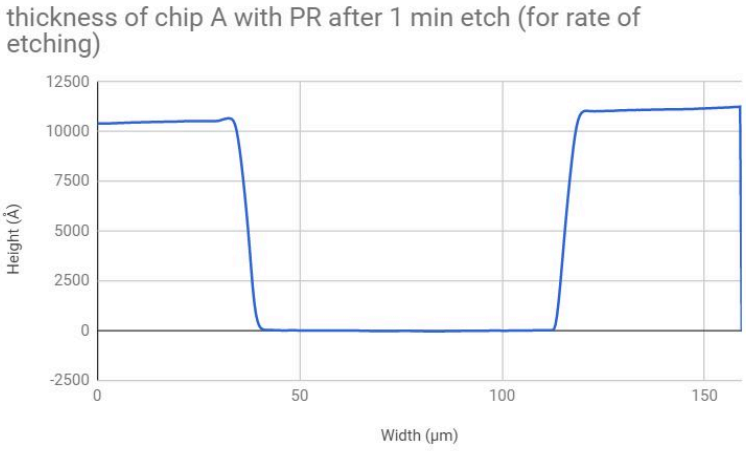


Figure 16: Photoresist thickness + etch depth after 1 minute

As shown in figure 15, we started with a PR thickness of around 10150Å and after etching the sample for 1 minute, the thickness measured totals around 11050 Å (Figure 16). This means we etched off (11050-10150) = 900 Å SiO_2 in one minute. For ~5600 Å SiO_2 and 20% overetching, we found that 9 minutes of etching was sufficient to get our future diffusion regions down to bare silicon.

To verify that we have etched off all SiO_2 in the desired region, we examined them under the microscope to compare the color with that of a pure silicon. As you can tell from Figure 17 below, the etched regions look white, which means bare silicon has been reached.

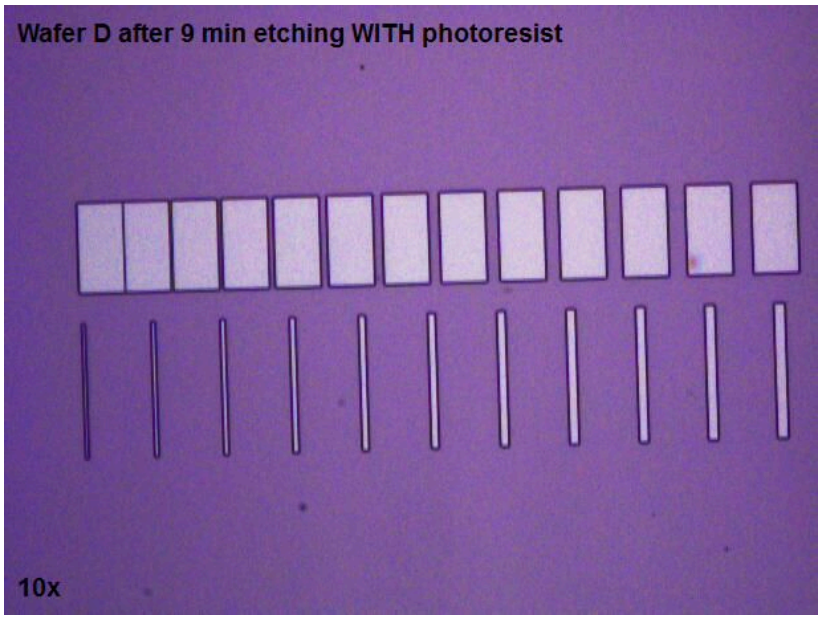


Figure 17: After 9 minutes of HF etching

We then removed the photoresist by dipping in acetone for 1 minute for initial removal, followed by a minute in acetone in a sonic bath, then another minute in 2-propel in the sonic bath. This is the procedure for every photoresist removal.

Day 3: Phosphorus predeposition, drive-in and field oxide growth

For our phosphorus predeposition, we used the PDS (planar diffusion source) PH-950 n-type solid sources. We prepared the wafers for the predeposition by going through the standard Ace-Iso-DI cleaning procedure and Piranha Clean, and then we put our samples in the phosphorus furnace for 15 minutes at 950 °C.

Figure 18: Bob Hill loading samples into the phosphorous furnace

After letting samples to cool, we used 50:1 DI H_2O:HF to remove the phosphorous glass layer formed on the surface of the substrate during the diffusion process. We started by dipping the test wafer B into 50:1 DI H_2O : HF for 5 minutes to see if water was beading on the surface as silicon is hydrophobic. Once we were satisfied that 5 minutes was enough, we dipped the rest of our samples for the same 5 minutes. After removing the phosphorus glass layer, we rinsed our samples in DI H_2O for 2 minutes and dried them off with N_2 gas. The sheet resistance on the test wafer is about 0.002542 Ω-cm.

Now we were ready to grow our ~2000 Å of wet oxide. We used the same procedure we used to grow the initial oxide layer to grow this layer, and in the end we had about 6000-6500Å of field oxide while the source and drain regions were covered by about 2000 Angstroms of oxide. Figure 19 shows our diffusion regions in our adder after the drive-in process.

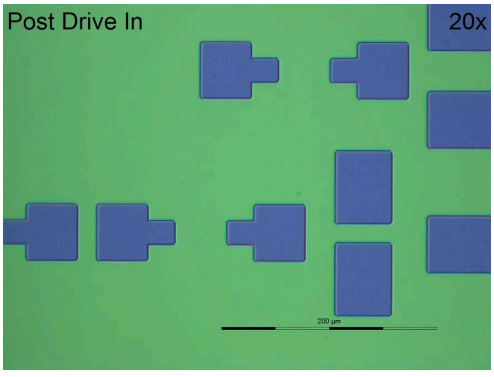


Figure 19: Diffusion regions after drive-in

Day 4: Gate Lithography using Mask-2 and gate oxide growth

We started with standard Ace-Iso-DI cleaning and dehydration bake. Then we placed the wafers under the HMDS vapor deposition hood for 3 minutes, spun photoresist on and soft baked for 1 minute. Then we aligned Mask-2 with Mask-1 and exposed under UV light for 12 seconds. After 75 seconds development in 4:1 DI H_2O:AZ 400K developer, we verified patterns under the microscope.

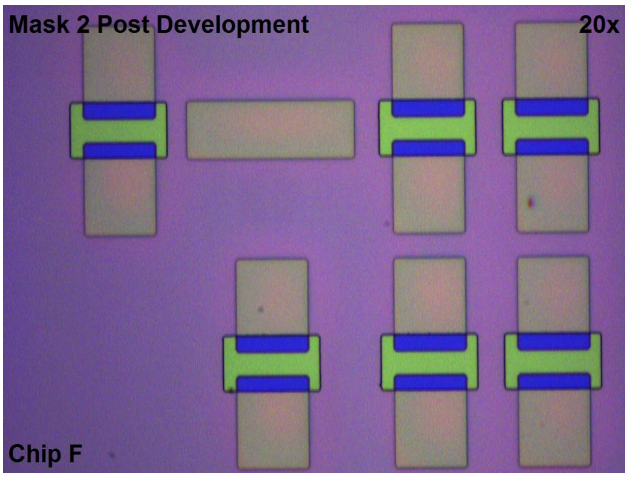


Figure 20: Mask 2 post development

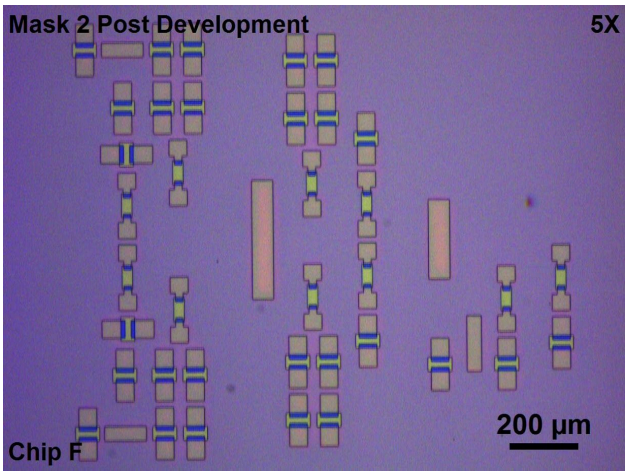


Figure 21: Mask 2 post development

Then we did an O_2 plasma descum and prepared for etching of the gate region. The etching rate was about 906 Å/min. We had to remove all of the oxide from the gate region, which had a thickness of about 6000Å. After etching away at chip B repeatedly until we felt all the oxide had been etched away with DekTak measurements in between, we decided that a 7 minute etch time was sufficient to ensure that we reached the silicon layer in the gate region with a 20% overetch. Figure 20 shows that we've etched away all the oxide. In order to make sure that we removed all the oxide in the gate region of our mosfets, we measured the difference between the source and drain oxide plus the thickness of the PR and the field oxide. Before we did any etching, this number was at around 8000Å (Figure (22)). After a few etching trials, our number stabilized at around 13200Å at 7 minutes (Figure (23)), which would put our field oxide at around 5200Å, which we deemed close enough to our expected figure of 6000Å. There are several factors that would have caused this difference between the actual and expected oxide thicknesses, including the formation of the oxide on our chips and systematic errors in the DekTak's measurements. Etch completion was verified by visual inspection for expediency.

We etched all of our chips for 7 minutes, then we stripped the photoresist from the chips and prepared them for gate oxide growth by performing a piranha clean and a brief HF dip.

Figure 22

Figure 23

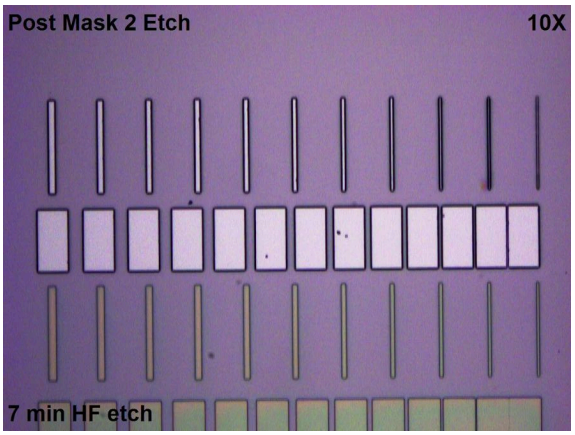


Figure 24: After mask 2 etch

Using the dry oxide growth procedure, we put the wafers into the furnace for around an hour and 15 minutes to grow around 400-500Å of gate oxide.

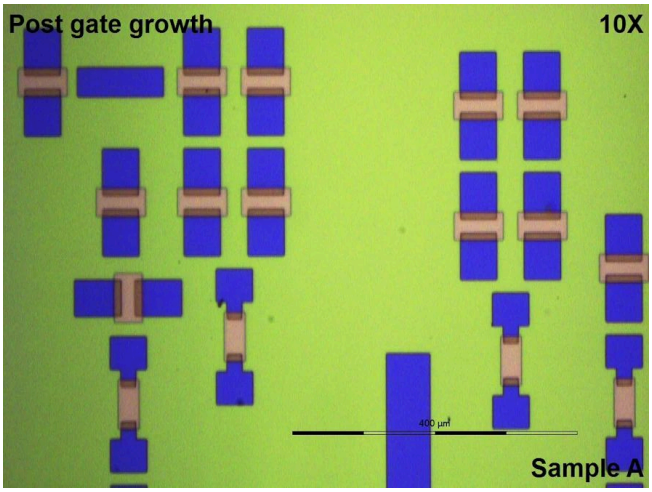
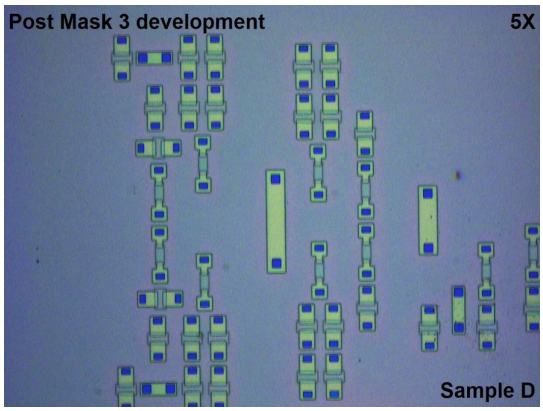


Figure 25: After gate oxide growth of 400-500Å

Day 5: Contact Lithography and Etching

After our gate oxide was grown, we transferred the pattern from Mask-3 (vias) onto the samples. We used standard lithography techniques to transfer the pattern, starting with a standard Ace-Iso-DI cleaning and dehydration bake, then placing wafers under the HMDS vapor deposition hood for 3 minutes, spinning photoresist on, and soft baking them each for 1 minute. We aligned Mask-3 with Mask-2 for each chip and exposed them to UV light for 12 seconds. After 75 seconds development in 4:1 DI H_2O:AZ 400K developer, we observed the newly formed patterns under the microscope. After development, the photoresist covered the gates

while a small sliver of the drain and source were left uncovered for the vias. Figure 25 shows where the vias are exposed for etching.



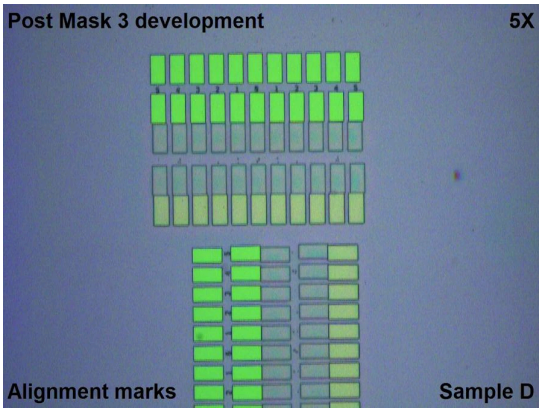


Figure 26: After mask 3 development Figure 27: Alignment marks after development

We knew that the oxide layer over the source and drain was around 2500Å: around 2000Å from after mask 2 and an added ~500Å from the gate oxide growth. We etched chip A repeatedly until we felt that all of the oxide from the exposed regions had come off, using both the microscope to check for color and the DEKTAK to get a numerical value. Figure (28) shows the thickness of the PR around the via. It's also worth noting that the difference between the PR on the left side and the right side is about 4000Å, which exists because of the 6000Å field oxide on one side of the drain/source and 2000Å on the other from the drive-in process. Figure (29) shows that after about 2.5 minutes of etching (Our initial approximation based on the ~900Å per minute etch rate found earlier), we had etched away 2130Å of oxide, and Figure (30) shows that another minute and 15 seconds, or 3.75 minutes total, of etching was enough to remove 2590Å of oxide, which is approximately the 2500Å of SiO_2 that we had estimated earlier.

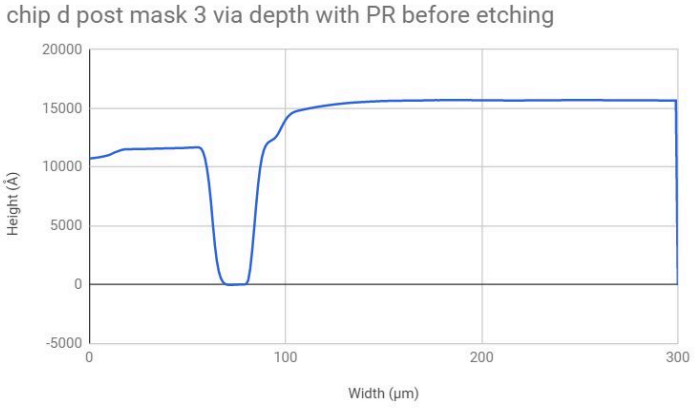


Figure 28

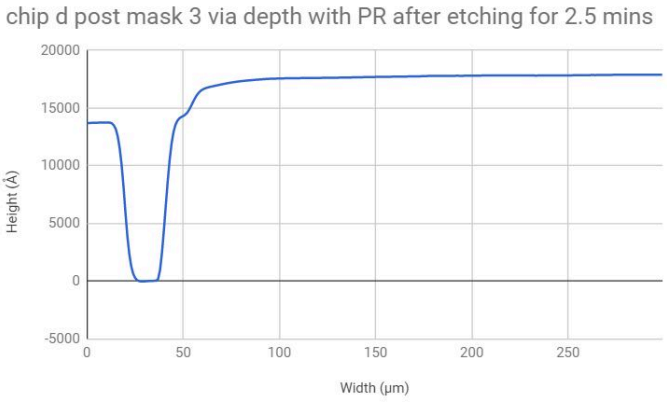


Figure 29

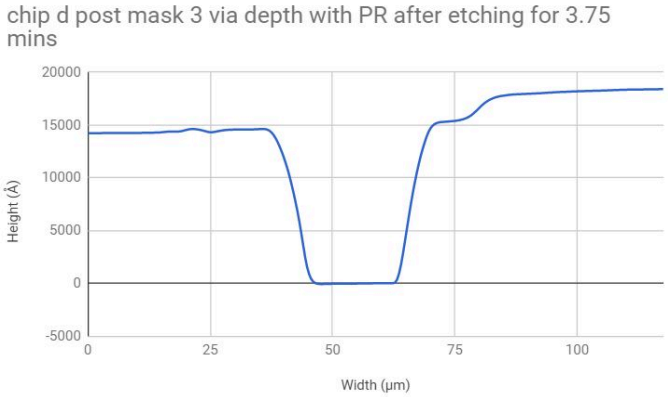


Figure 30

We were satisfied with this number and you can see in Figure (31) and (31) that those regions in the source and drain and TLM resistor left exposed by Mask 3 were white under the microscope, though we had an incident with the white balance that caused the white parts to look not-so-white in the photo. Visual inspection moments before proved the vias to be very white.

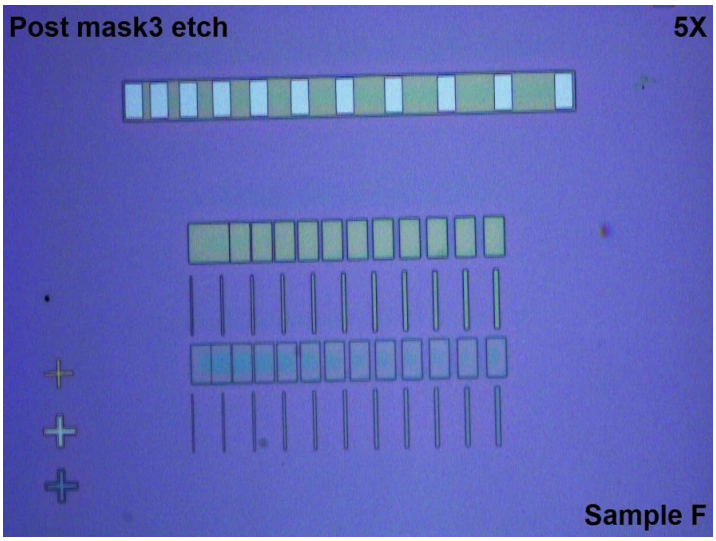


Figure 31: After mask 3 etch

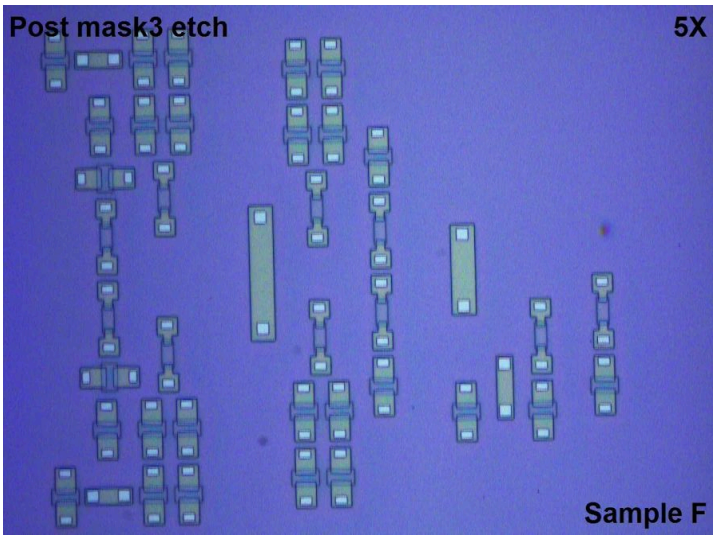


Figure 32: After mask 3 etch

After fully etching away the oxide from the exposed regions of the source and drain, it was once again time to remove the old photoresist and prepare it for another layer for Mask-4. This was done with the standard Ace-Iso-DI cleaning and dehydration bake, then placing wafers under the HMDS vapor deposition hood for 3 minutes, spinning photoresist on, and soft baking them each for 1 minute. At this point, the mask alignment process was pretty familiar to us and it didn't take long to apply Mask-4 to our chips. As this final mask was for the metal liftoff step, before we could develop our photoresist we had to dip the samples in a toluene solution for 5 minutes. This is done to harden the outer layer of the photoresist so that when we develop it, it creates a slight lip at the top of the photoresist profile, which is useful as the metal cannot cover the side walls as easily and metal liftoff is significantly neater. However, initially breaking down the strengthened outer layer is a little harder for the developer, so we had to develop our samples for a slightly longer time of 115 seconds, as opposed to the ideal 75. Now with Mask-4 applied and the toluene creating an a nice lip in the photoresist to reduce step coverage, we were ready for the metal deposition and lift-off process.

Day 6: Lift-Off Lithography and Metallization

To start this day, we did a quick 50:1 DI H_2O:HF dip before putting the wafers in the metal evaporator. We prepared the evaporator to evaporate 3000 Å of aluminum onto the surface of the wafer and loaded the samples. Pumping down to mid 10^{-6} torr, around 3000 Å of aluminum was deposited. Once the evaporation process was complete, we were ready for the lift-off of the metals to complete our semiconductor. We had ensured the side wall profile of the photoresist was set for a proper lift-off when we had done the toluene dip. To perform the metal lift-off, we

placed the wafers in acetone overnight to properly lift-off the PR under the metal. When we came back the next morning, we used a pipette to jet acetone at our chip, agitating the PR to come off along with the undesired aluminum resting on top. We dipped the sample in ISO and DI and blow dried with $N_{2,}$ after which we were ready to begin testing our devices. You can see where the metal was lifted off in the figure below.

Aluminum Removal

Figure 33

Device Characterizations

To test our devices, we began by TLM contacts in order to see if they were ohmic. For our device, they were ohmic so we did not have to sinter the contacts on the strip annealer. We measured the contact resistance of the ohmic contacts and various I-V curves in order to determine the transconductance, threshold voltage and various other characteristics of the devices that we had fabricated.

Resistance Testing:

The slope of each IV curve that we measured for the resistors has a slope of 1/R, due to the equation $I = \frac{1}{R}(V)$. In order to measure the resistances of each resistor, we used the inverse slope of the I-V curve.

Circuit Intent:
Our circuit is a full-adder, which is a circuit that takes 3 inputs (2 manual inputs and a carry-in bit) of either high or low signals and then adds them together using binary algebra, with the outputs being the sum and the carry-out bit. In order to do this, we needed 2 XOR gates, 2 AND gates, and a single OR gate put together in this arrangement:

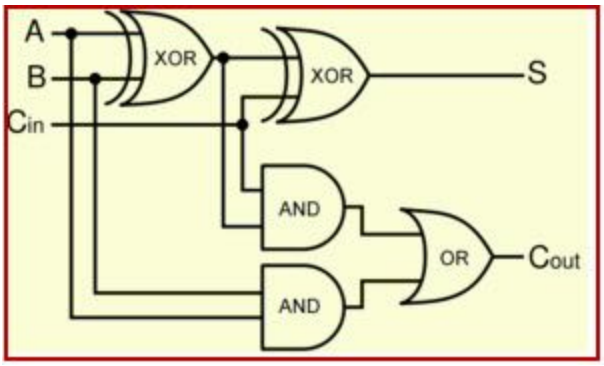


Figure 34

We also had individual XOR, AND, and OR gates on our chips so that we could prove that they worked separately before testing the full adder where the 4 gates would have to interact with each other.

In order to prove that our gates and full adder were working, we used a testing method where we would hold one input at a high or low value (0V or 19V) and swept the other input from -19V to 19V. The reason we decided to test our gates and adder this way was because of the truth tables of each of the gates and the adder. This can be easily illustrated using the truth table of an AND gate as an example:

Input 1	Input 2	AND Output
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: AND gate truth table

In Table 2, we can see that for an AND gate, if Input 1 is kept at 0 V and Input 2 is swept from a logical low to a high (-19V to 19V for our tests), the output should stay at a logical low, regardless of the sweeping voltage from Input 2. However, if Input 1 is kept high while Input 2 sweeps from low to high, the output of the AND gate should follow Input 2, transitioning from low to high when Input 2 has reached a voltage considered a logical high. It is easy to see how this is a very effective way of testing the characteristics of a logic gate, as it shows how the outputs react to varying inputs, that the gate is operating correctly, and at what voltage the input is high enough to have an effect on the output (when the voltage is considered a logical high). This method is just as easily applied to both XOR and OR gates by seeing how the outputs change when input 2 sweeps from low to high and input 1 is kept at either a logical high or low voltage.

Input 1	Input 2	OR Output
0	0	0
0	1	1
1	0	1
1	1	1

Table 3: OR truth table

Input 1	Input 2	XOR Output
0	0	0
0	1	1
1	0	1
1	1	0

Table 4: XOR truth table

As mentioned above, this method can also be used to test a full adder if we know the adder's truth table. The truth table for a single full adder is as follows:

Input 1	Input 2	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 5: Full Adder Truth Table

We can see that for a full adder, we have 3 inputs, making the truth table 8 rows long. However, this doesn't change our testing method. The first test would be to have input 1 and 2 at 0 V while sweeping the carry-in bit from a logical low to a high. The result of this test should be that the sum follows Cin as it becomes a logical high while the carry out bit should remain low. The second test is where Input 1 is kept at 0 V while Input 2 is held at 19V and Cin is swept from a logical low to a high. The sum should move from a logical high to a low while the carry-out bit transitions from a low to a high. The third test is where we make Input 1 19V while Input 2 is set to 0V. Sweeping Cin the same way should yield the same results in the Sum and Carry-Out bits as in the previous test. The final test is where both inputs are held at a high voltage while the carry-in bit is swept, in which case the Sum bit should move from a low to a high and the Carry-Out bit should stay at a logical high. If our full adder circuit followed this behavior, we could prove that it, along with the 4 individual gates, was behaving as it should.

DATA ANALYSIS:

CIRCUIT TEST RESULTS:

AND:

Input 1	Input 2	AND Output
0	0	0
0	1	0
1	0	0
1	1	1

Table 1: AND gate truth table

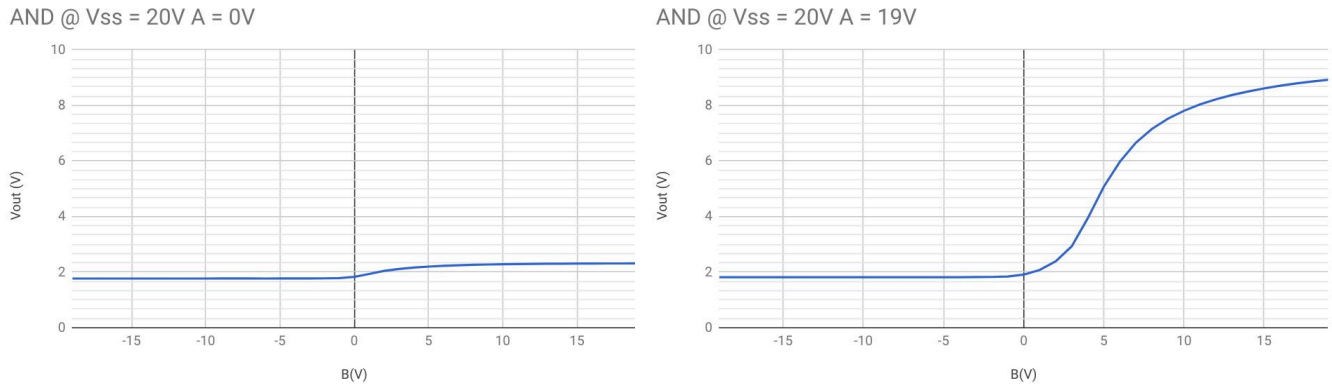


Figure 35

Using the testing method mentioned above, we were able to get these two plots. Input B was swept from -19V to 19V and we just changed Input A from 0V to 19V. Using the truth table as reference, if we keep A at 0 while sweeping B, the output should remain low, and we can see that it does from the graph on the left. When testing with Input A as a high 19V, the output should transition from low to high, as one can tell that it does from the graph on the right. Using this data, we were able to prove that our AND gate was working properly. From Figure 35, we can read that the output low for AND gate is 2.33V, and the output high is 9V.

OR:

Input 1	Input 2	OR Output
0	0	0
0	1	1
1	0	1
1	1	1

Table 2: OR truth table

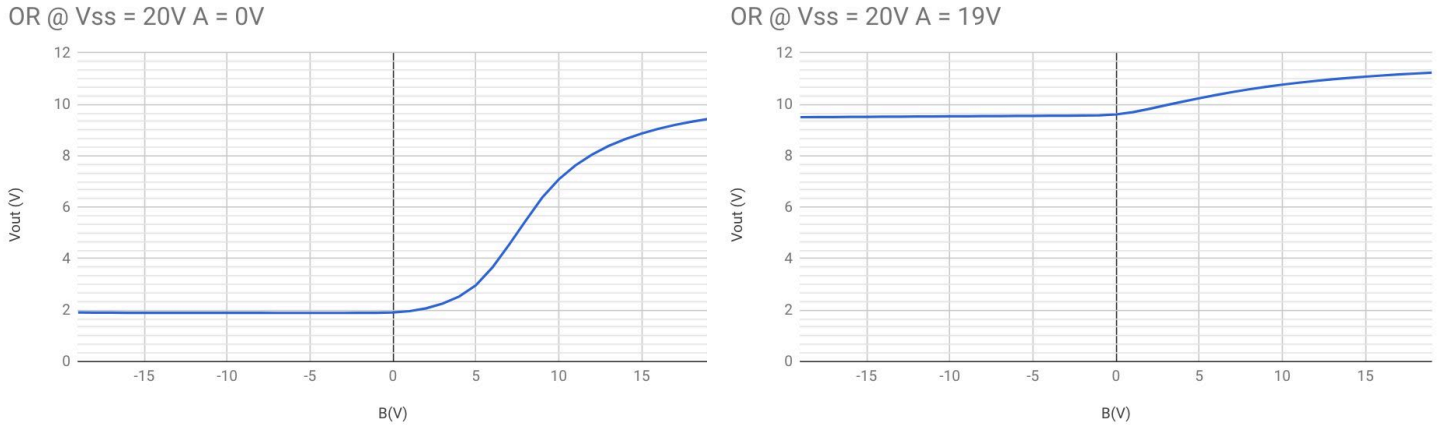


Figure 36

For the OR gate, testing procedure was the same as used for testing the AND gate. Using the truth table as reference, if we keep A at 0 while sweeping B, the output should transition to high with B, and we can see that it does from the graph on the left. When testing with Input A as a high 19V, the output should remain high, as one can tell that it does from the graph on the right. Using this data, we were able to prove that our OR gate was working properly. From Figure 36, we can read that the output low for OR gate is 1.89V, and the output high is 9.33V.

XOR:

Input 1	Input 2	XOR Output
0	0	0
0	1	1
1	0	1
1	1	0

Table 3: XOR truth table

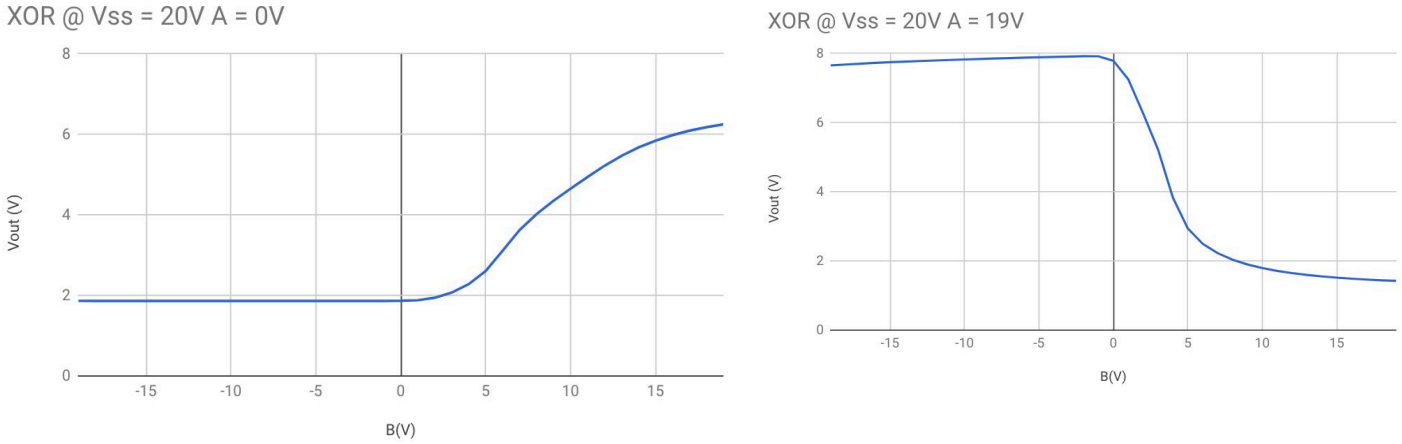


Figure 37

Following the same testing procedure and using the truth table as reference, if we keep A at 0 while sweeping B for our XOR gate, the output should transition to high with B, and we can see that it does from the graph on the left. When testing with Input A as a high 19V, the output should drop to a logical low as B becomes high, as one can tell that it does from the graph on the right. This data proves that our XOR gate is working as intended. From Figure 37, we can read that the output low for AND gate is 1.8V, and the output high is 6.2V.

We did, however, have a lot of trouble testing our XORs. This was due to two main reasons. The first reason was that we made a mistake in our mask design where we failed to ground one of our MOSFET sources. At first, we tried to wire bond the dangling source to a nearby ground, but the technique was too difficult for us to learn on the spot and we ended up ruining the contacts of every gate we tried it on, not to mention that it didn't work at all. In the end, we added an extra grounded testing pin to contact with that source so that it would still be grounded. The second problem that we had was with the sweeping of Input B. Though we didn't initially know what the problem was and just tried testing every XOR gate that we had made, switching the testing pins, and ensuring that we were making good contact, we later found out that our sweeping speed was too fast for the output to display a concrete curve. Because the XOR gate was the most complex of our gates, the signals didn't have enough time to travel through our circuit and generate an output before the input changed. To solve this problem, we set delay and hold times to 1 second so that the signals would have time to traverse the circuit and we would get a good output curve.

FULL ADDER:

Input 1	Input 2	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4: Full Adder Truth Table

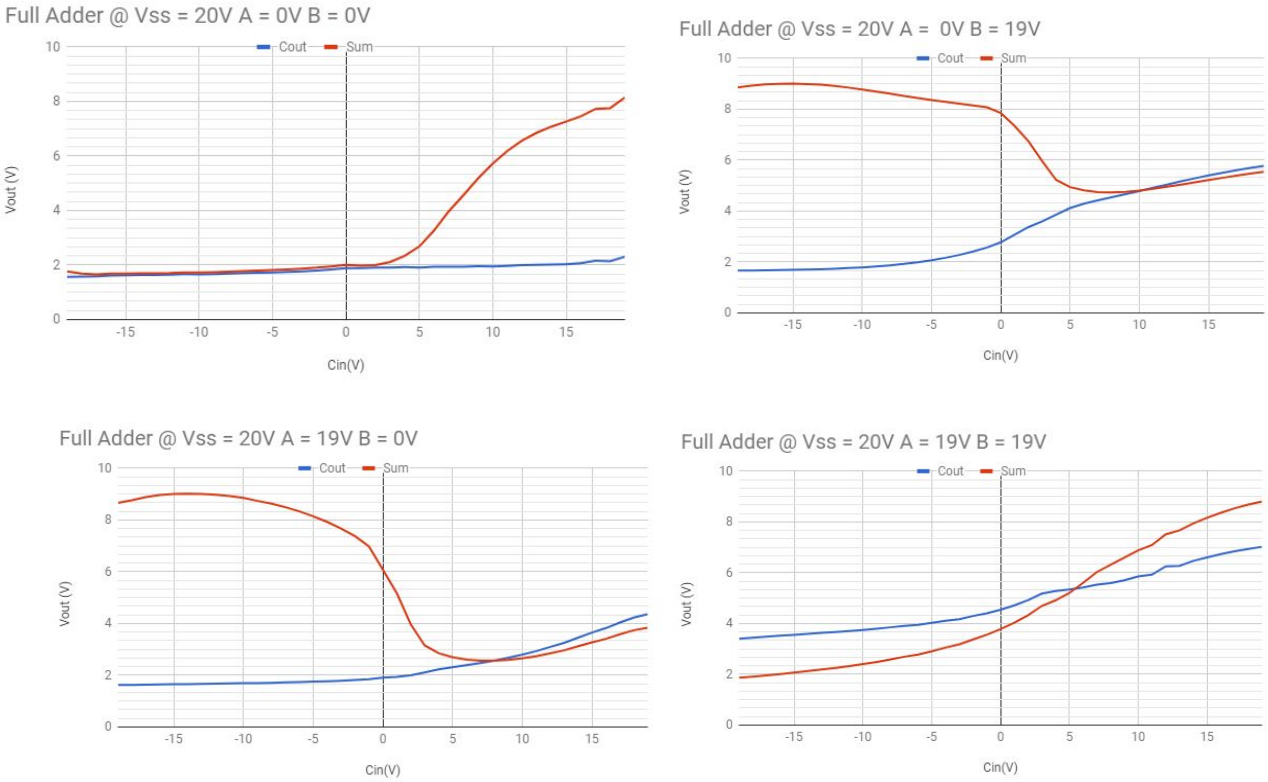


Figure 38

These are the results of our tests on our full adder. We used the testing method that we decided on for testing full adders mentioned previously.

The graph on the top left shows the Sum and Carry-Out outputs when inputs A and B were held at 0V while Carry-In was swept from -19V to 19V. According to the truth table, this should

make Sum transition from a low to a high while the Carry-Out bit stays low, which we can see that it does.

The graph on the top right shows the outputs when input A is held at 0V and B is held high at 19V. From the truth table, we can see that the Sum should go from high to low, while Cout goes from low to high. However, in our graph you can see that our Sum starts high as it should but doesn't really drop down to a true low, instead following the Cout curve slight upwards, just below it. The Cout also doesn't make a great increase, going from just under 2V to just under 6V.

The bottom left graph, which shows the outputs when input A is high and B is low, should technically be the same as the top right graph as both inputs go through the same number of gates (refer to figure 38), but due to the locations of our inputs on our actual chips, propagation times are different between the inputs and the output did vary a little bit. In this graph, you can see that the Sum makes a nice dip to a low, but Cout barely moves up, going from just under 2V to just over 4V. Also, notice that the Sum again curves up after hitting the low to follow Cout, just under it. We don't exactly know what causes this interesting behavior, but we think it may be due to leaky voltage.

The bottom right graph shows output behavior when both inputs are held high at 19V while the Carry-In bit is swept from low to high (-19V to 19V). The truth table shows that in this instance, Sum should go from low to high while Cout stays high. Our graph shows that the Sum makes a strong transition from around 2V to 9V, but the Cout moves from just under 4V to around 7V. We believe that Cout's curve starts at a high enough voltage to be considered as starting high, but the Carry-Out bit's movement in all of our tests were pretty unimpressive compared to our Sums. We believe that this is due to the fact that signals must travel much further to get to Cout than Sum, and must go through 4 gates total, as opposed to the 2 gates signals must go through to get to Sum.

Regardless of the quality of our results, we think that our full-adder worked rather well. After running many tests on practically all of our gates and adders, we think that the threshold voltage between a high and low signal lies somewhere around 3V, and our full adder technically performed correctly under this assumption. However, we do not have the expected high and low outputs of our full adder as load line analysis is far too complex with all of the gates and a non-linear element, the diode, as our load. We are very satisfied with our results as we were concerned that with so many gates and wires in our circuit, we would have very little room for fabrication errors, and any major mistake would have caused us to not be able to get any readings from our adder or any of the gates. While the less than ideal performance of our adder was most likely a fabrication error anyway, we are glad that the time spent in the lab tediously making sure that every feature on our chips was accurately formed was worth it.

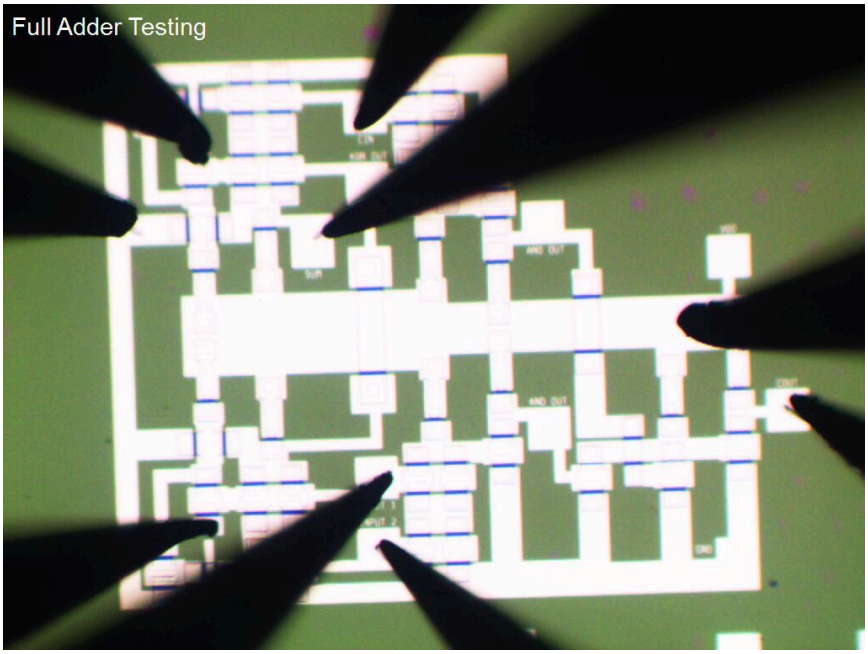
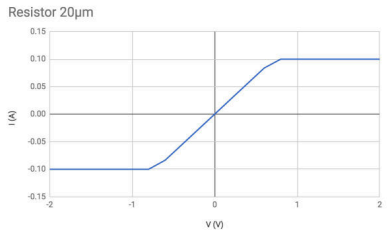
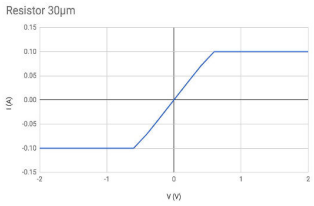
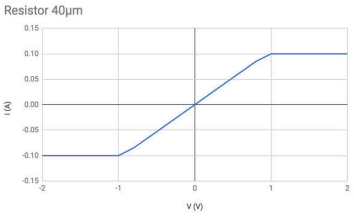
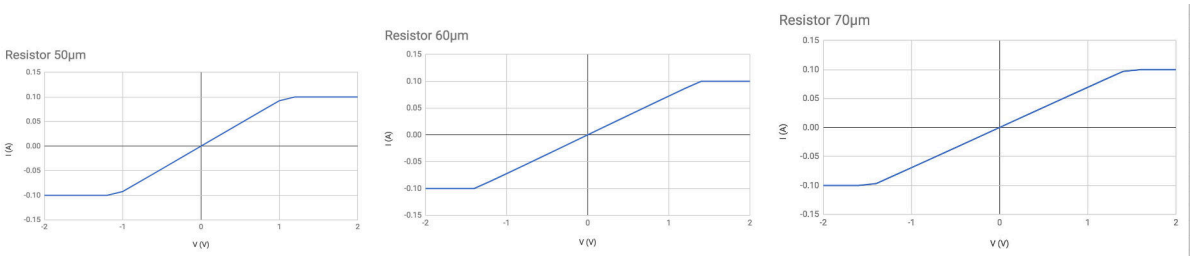


Figure 39: FA testing with 9 pins

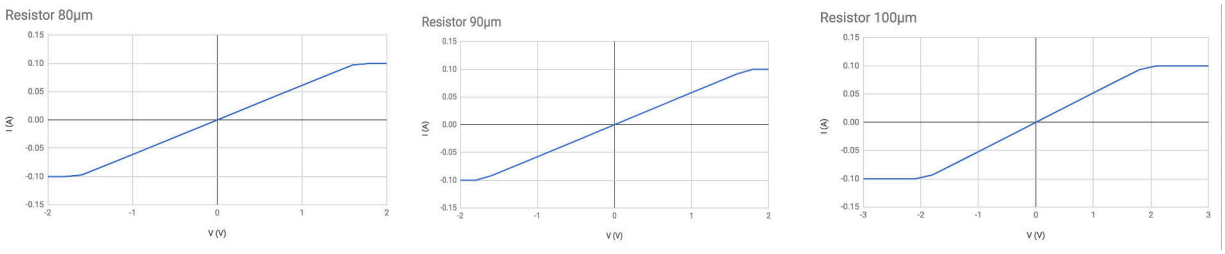
TLM:

20 um x 100 um	30 um x 100 um	40 um x 100 um
		
R = 0.6V/0.0839A = 7.15 Ω	R = 4V/0.702A = 5.7 Ω	R = 8V/0.849A = 9.42Ω
50 um x 100 um	60 um x 100 um	70 um x 100 um



R = 4V/0.371A = 10.78 Ω R = 10V/0.724A = 13.8 Ω R = 12V/0.831A = 14.44Ω

80 um x 100 um 90 um x 100 um 100 um x 100 um



R = 14V/0.853A = 16.41Ω R = 16V/0.92A = 17.37Ω R = 19V/0.778A = 19.28Ω

Figure 40

Resistance vs Length

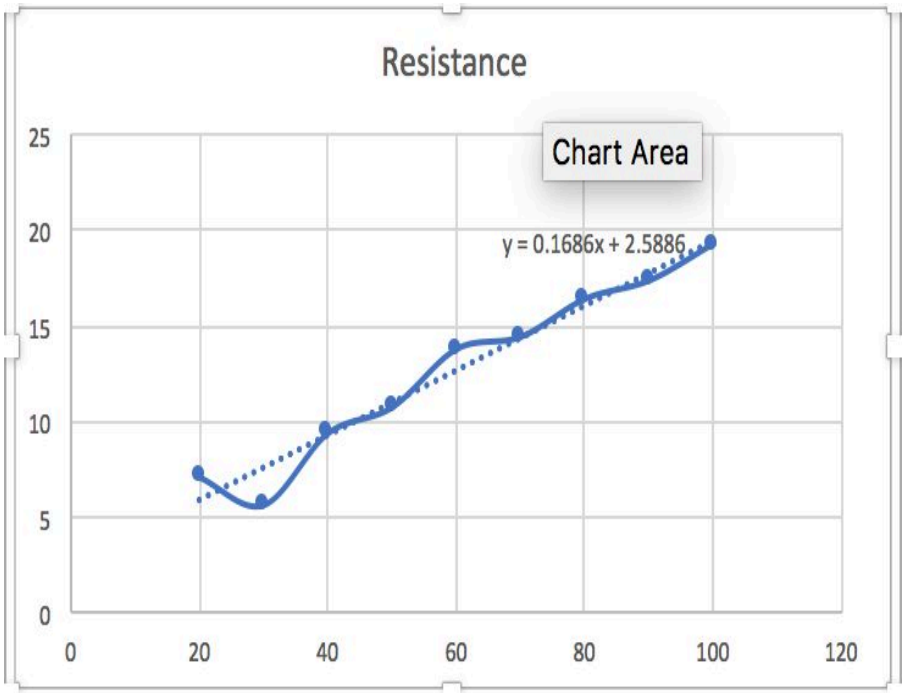


Figure 41

Using the resistance values found from the measured IV curves, we plot a graph of length vs. resistance to see the linear rise in values (as length increases → the resistance increases). The point where the trend line intercepts the y-axis is equal to $2*R_{contact}$. We can see that the value is 3.672 Ω, therefore our contact resistance is equal to 2.5886 Ω/2 = 1.2943Ω.

Sheet resistance = (slope of the R vs. L curve) * Width

$$= R_{sheet} = \frac{R}{L}W = 0.1686\frac{\Omega}{um} \cdot 100\ um = 16.86\Omega/sq$$

From this information, we can see that resistance increases as the length L increases, as equation 1 states. However, our calculated sheet resistance does not plug into the equation to give us the correct resistance that we found, nor does the sheet resistance seem to stay constant. This is most definitely a fabrication problem, and while it might have been better on another chip, when we were taking data, we saw linear curves and assumed that the values were right.

$$R = \frac{\rho}{t}\frac{L}{W} = R_s\frac{L}{W},$$

Equation 1

MOSFETS:

$$C_{ox} \equiv \frac{\varepsilon_{ox}}{t_{ox}}$$

where $\varepsilon ox = 8.85 * 10^{-12} * 3.8$ for SiO2. Using 450 Angstroms as our oxide thickness, we get Cox = 0.07473.

Electron mobility = gd/[(Z/Lg)*Cox*(Vg-Vth)

Output conductance Gd = $\lambda \cdot I_{DS}$, λ = 1/(*early voltage*), as the early voltage is the x-intercept of Vd vs. Id curve

For the following data, we assumed that the threshold voltage occured at I_{DS}=100 uA.

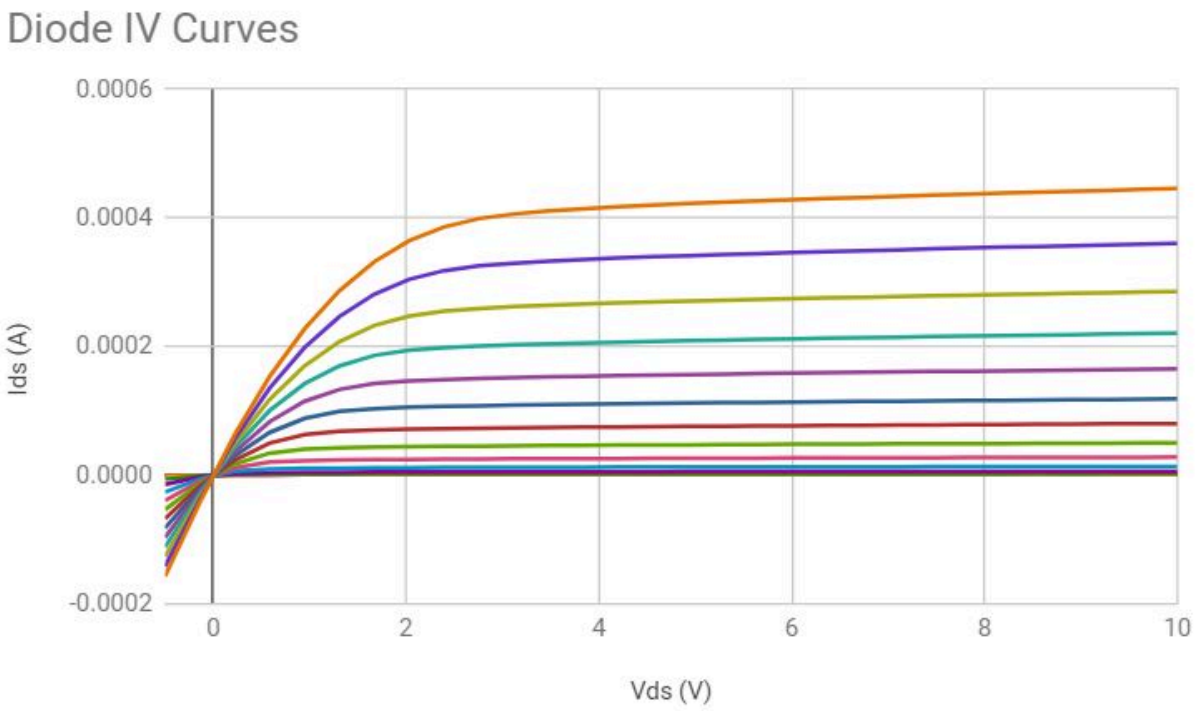


Figure 42

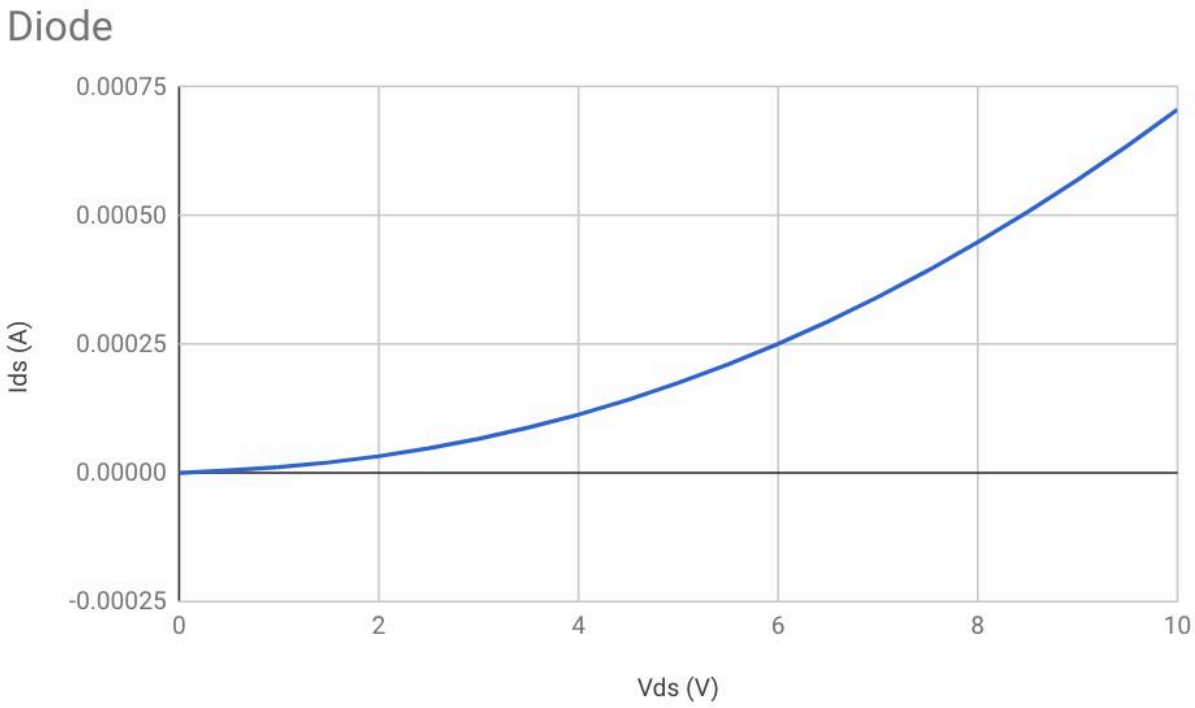


Figure 43

Transconductance=0.0706mS

R_{diode}=1/gm=14164Ω (ideally)

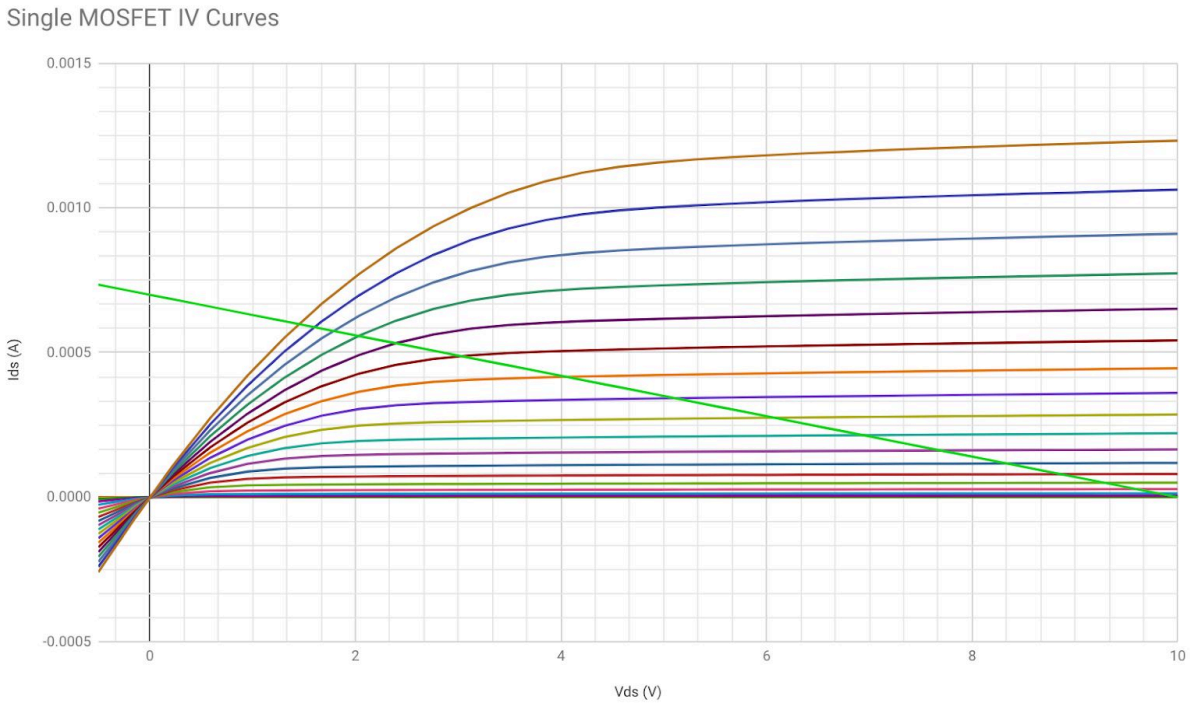

Single MOSFET IV Curves
0.0015
0.0010
0.0005
0.0000
-0.0005
Ids (A)
0
2
4
6
8
10
Vds (V)

Figure 44

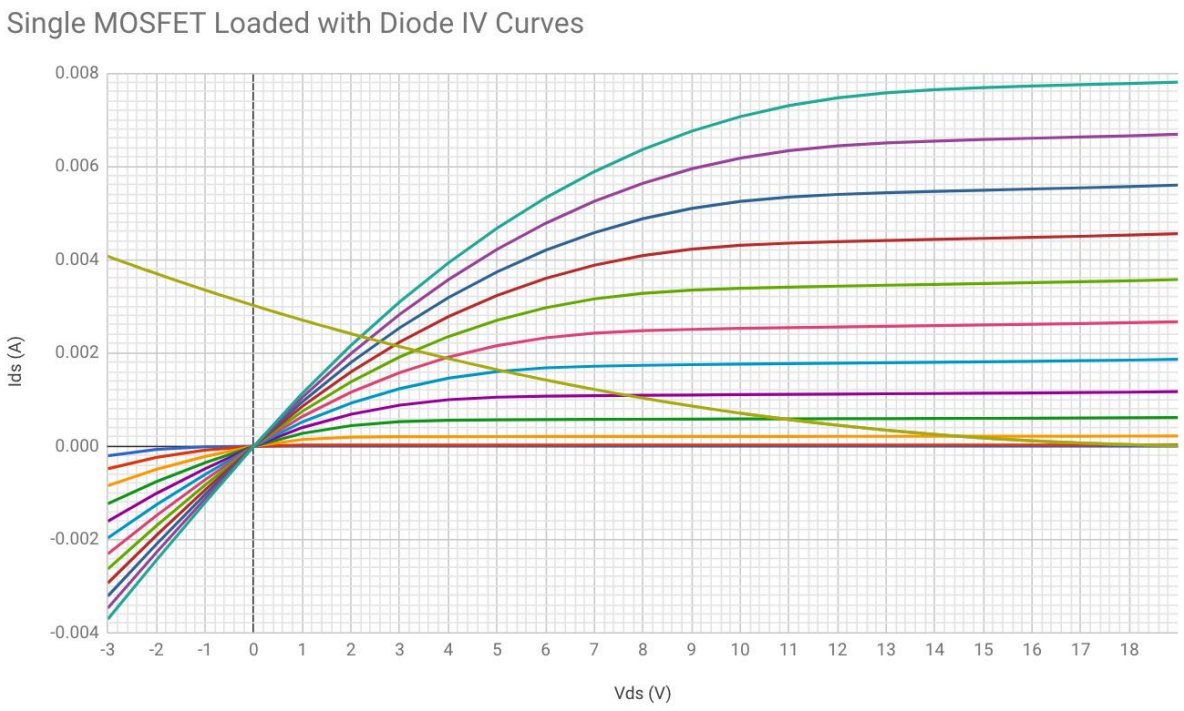


Figure 45

Channel Conductance gd = slope of Ids vs. Vds curve

At Vg = 0V, gd = 0 (mosfet is in cut-off)

→ At Vg= 1V, gd = 0.1015 mS

→ At Vg= 2 V, gd = 0.14 mS

→ At Vg= 3 V, gd = 0.198 mS

→ At Vg= 4 V, gd = 0.242 mS

→ At Vg= 5 V, gd = 0.31 mS

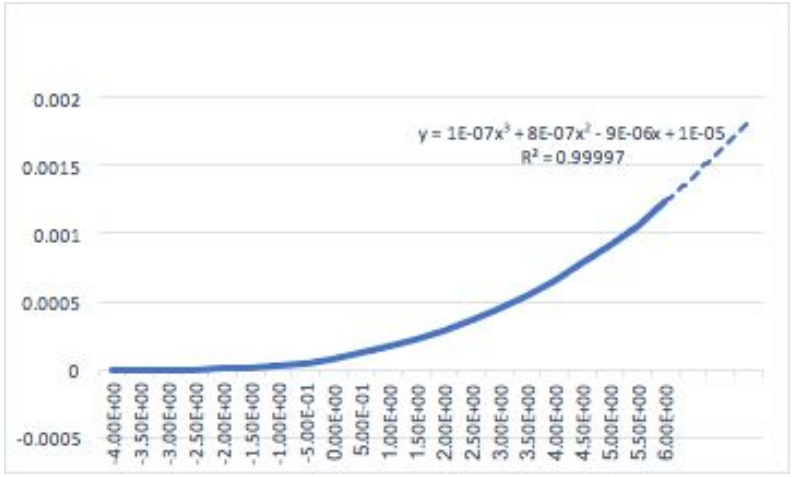


Figure 46: Ids vs Vg @ Vds 10V

We can get the Vth from the graph. We assumed that the threshold voltage occured at I_{DS}=100 uA and Vgs = 10V. From the graph we can see that Vth is about 0.24 V for our single MOSFET.

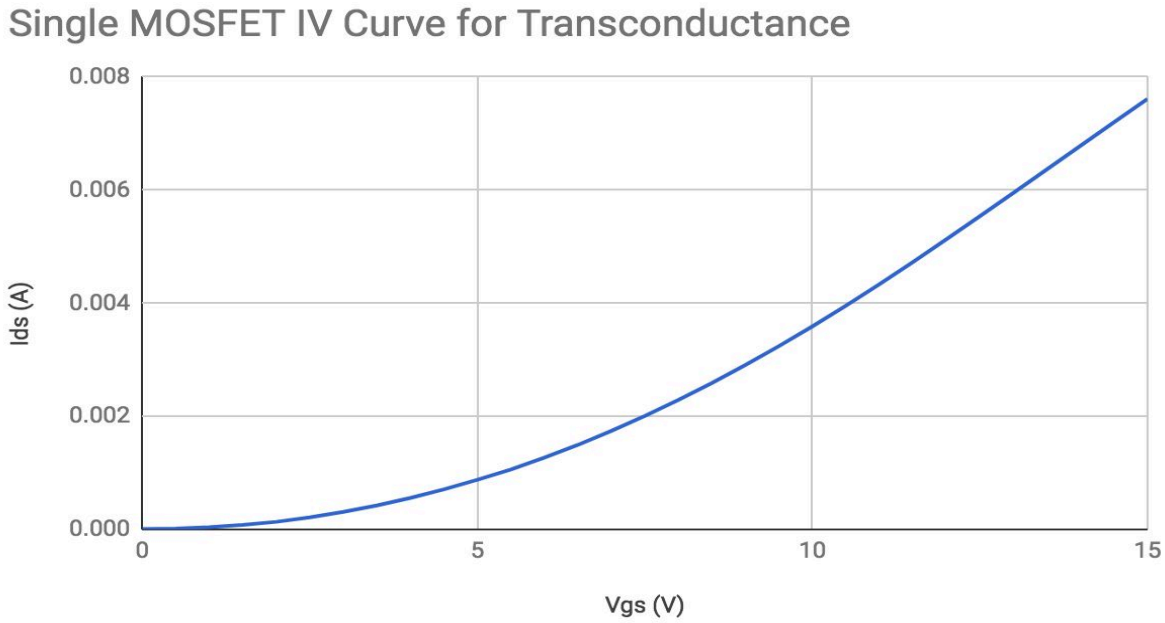


Figure 47

Transconductance gm = slope of Ids vs. Vgs curve=0.5 mS
ON resistance= 1/gm= 2000Ω

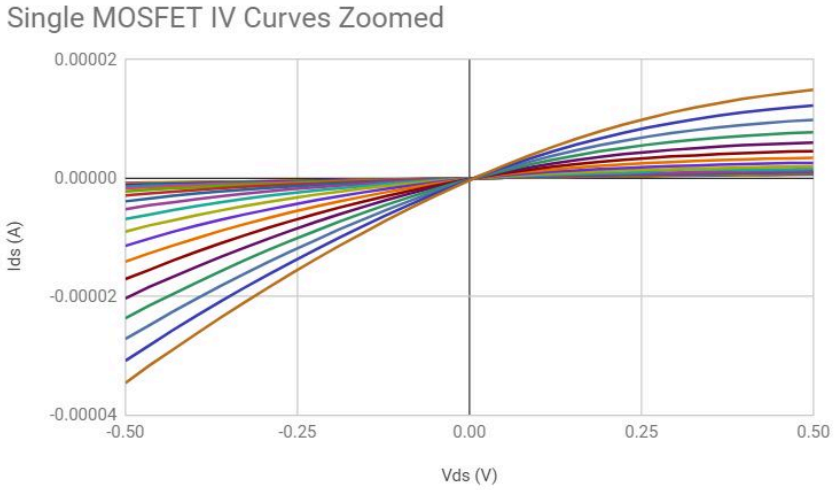


Figure 48

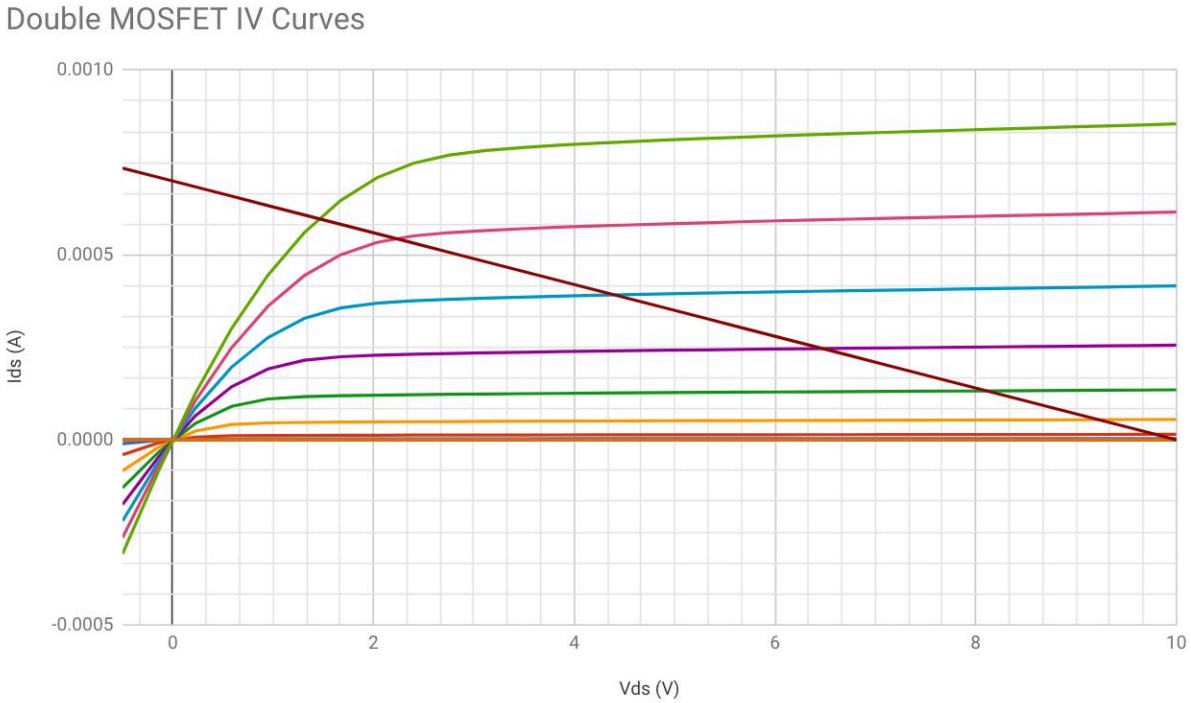


Figure 49

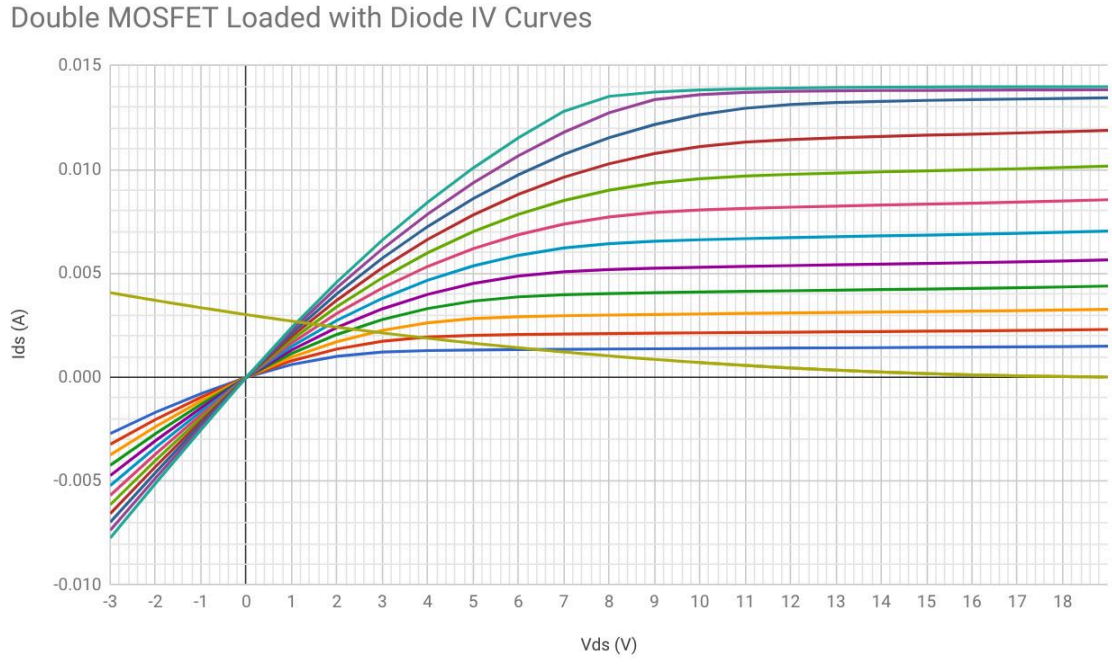


Figure 50

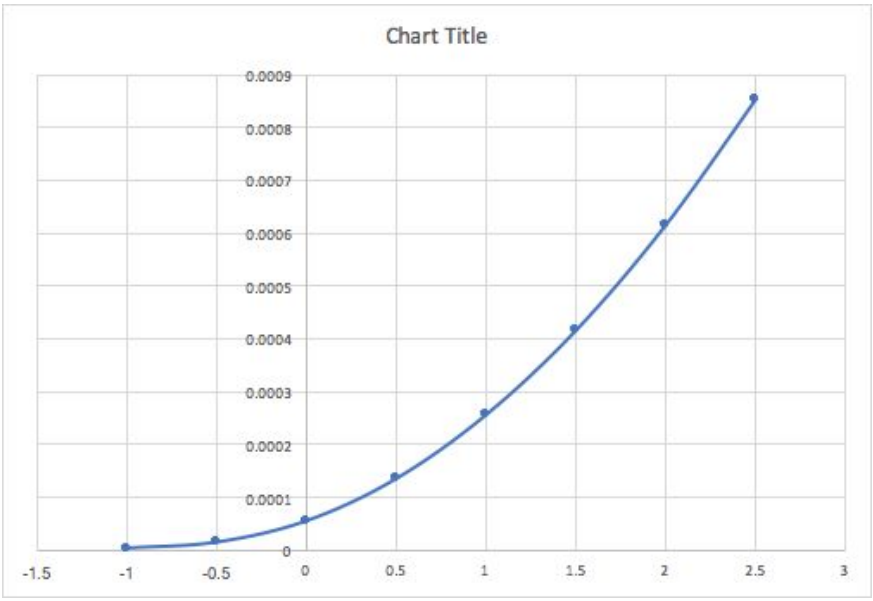


Figure 51: Vg vs Ids @ Vds=10V

We can get Vth of the double MOSFET from the above graph. We assumed that the threshold voltage occured at I_{DS}=100 uA and Vgs = 10V. From the graph we can see that Vth is about 0.3 V for the double Mosfet.

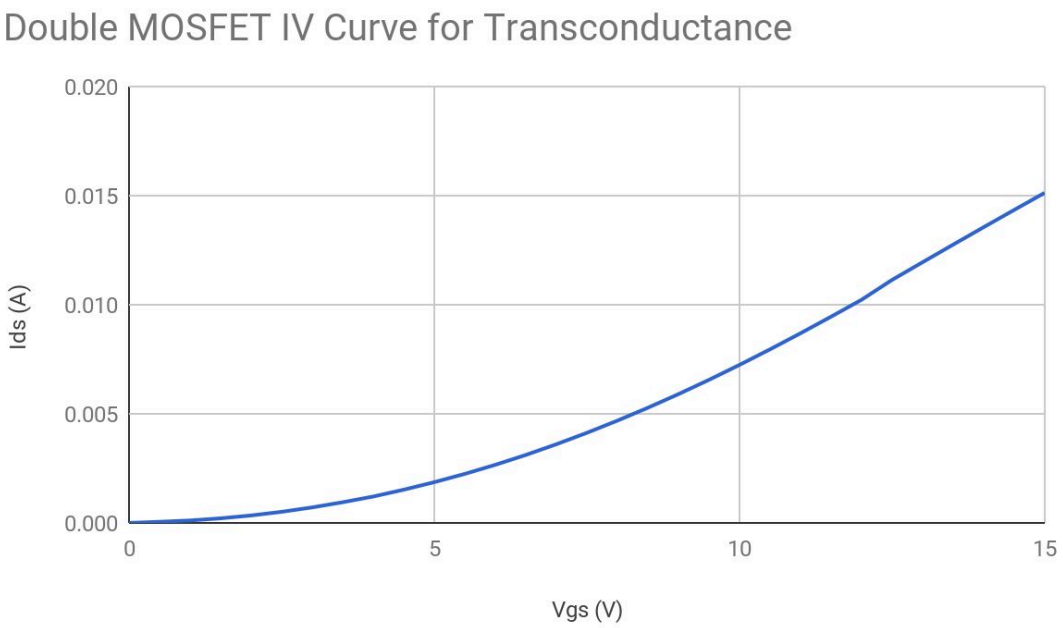


Figure 52: Ids Vg Vds @ Vds 10 V

Transconductance gm = slope of Ids vs. Vgs curve=1 mS
ON Resistance= 1/gm=1000Ω
Notice that this is half of the ON resistance of the single MOSFET as this MOSFET is two of the single MOSFETs in parallel.

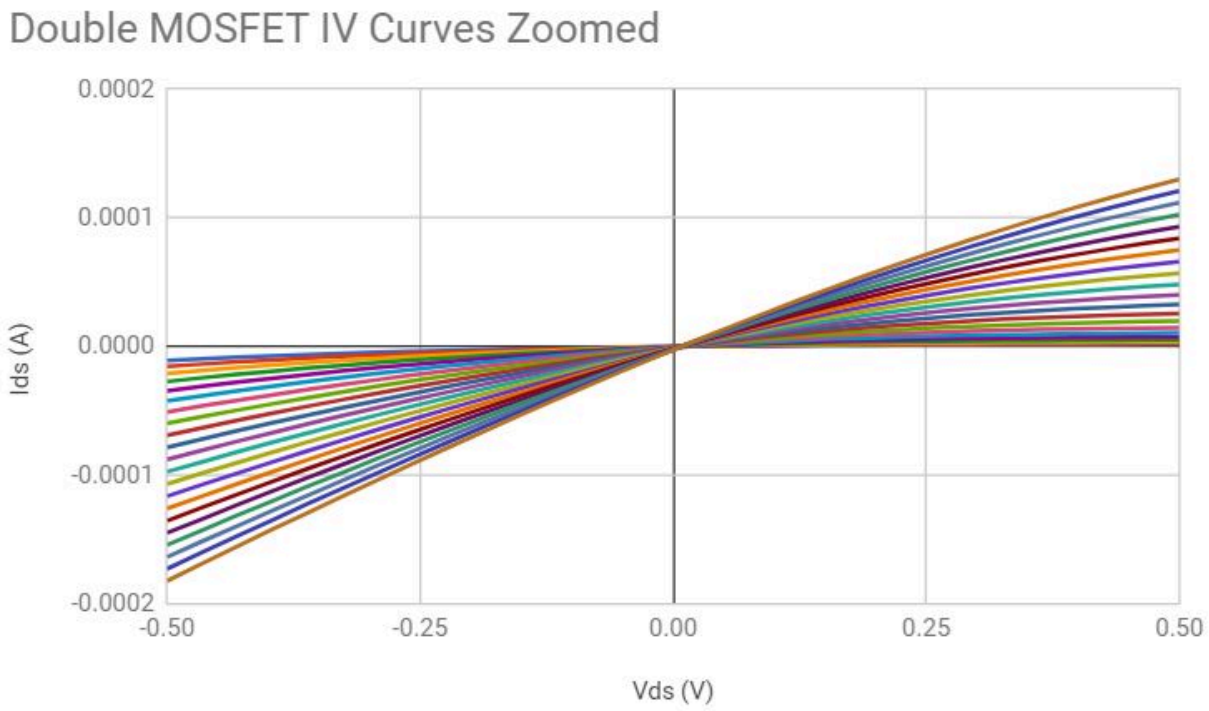


Figure 53

For both of the MOSFET, input low is 0V, while input high is 10V. Since we are using diode as resistor, our R_{on} should be 14164Ω ideally, and therefore the starting point for the load line should be Ids=0.0007A=700uA. For the single MOSFET the output low is 1.68V and the output high is 10V (read from Figure 44). For the double MOSFET the output low is 1.65V and the output high is 10V (read from Figure 49). However, in the real circuit, since we are using diode instead of a resistor, the load line should no longer be a straight line, for the resistance of a diode changes when we sweeping the voltage across it. So we plot new load lines based on the IV plot of our diode (Figure 45 and Figure 50). From the new load line, our new output low and output high for the single MOSFET is 2.2V and 18.4V. And the new output low and output high for the double MOSFET is 1.1V and 3.9V.

The calculated output low value for OR gate is 2.3V, which is smaller than the testing value, while the calculated output high value for OR gate is 10.8V, which is very close to our testing value. For both AND gate and XOR gate, the calculated output low is 1.1V, and the output high is 2.0V, which are not consistent with the testing values. We think this caused from using wrong load lines for calculation. Notice that in the real logic circuit, the diodes are never connected with a single or a double MOSFET alone. For the double MOSFETS, the diodes are always connected with two double MOSFETS. Since we are only measuring the diodes with one double

MOSFETS, the output voltage observed was lower than we expected. The OR gate calculation performs better, because it is more simple than the other two gates.

Capacitances:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

Equation 3

where ε_0= 8.854 pF/m, ε_r= 3.9 for SiO_2, A = area of capacitor, and d= thickness of oxide layer

For 1000 µm x 1000 µm capacitor:

$$C = \frac{8.854 \cdot 10^{-12} F/m * 3.9 * (1000 \cdot 10^{-6} m)^2}{450 * 10^{-10} m} = 767.3\ pF$$

The capacitor we built didn't work as expected. This was most likely due to a design problem before we even submitted our designs to be made into masks. The measured capacitance was about 9 pF, a negligibly small number. The problem is probably cause from the tolerance between bias and metal layers. We only leave 5um for the tolerance, which might be too small.

Conclusion

We started this lab by designing our own chip. It was a new experience and asked us to fully understand the structure of MOSFET, resistor, capacitor, the TLM, and alignment structure, because we need to design them layer by layer, and arrange all the structures properly. One important thing we found out in this procedure was to leave the testing pad big enough, and this made our life more easier when we started testing. We made a small mistake in this procedure which was forgetting to number the mask, and therefore we had to distinguish them one by one under the microscope when we were using them.

This lab was centered around using the skills and techniques we perfected over the course of the quarter to build and test our own MOSFET device from scratch. This process involved knowledge of many procedures, such as photolithography, mask alignment, dry and wet oxide growth, etching, plasma descum, Dektak oxide growth measurement, cleaning with piranha solution, metallization, and metal lift-off. With all of these tools in our arsenal, we were able to grow, layer, and etch oxide in patterns according to three masks to create a silicon wafer with defined channel, source, and drain oxide.

We originally started off with six chips, but after the fist mask we lost chip B because of over etching. Executing the project itself was nearly seamless, with problems easily erased by

repeating a cleaning step or adding time to an etch to achieve desired results. By constantly checking our work with the Dektak and other tools, we were able to quickly catch and mitigate problems. While we did experiment with development and pre-deposition times, our results appeared to be consistent.. Another issue occured when we measured our devices/ We failed to receive the output for our XOR gate, and we found out that was because we forgot to ground one of the MOS in our design pattern. Fortunately, this error was solved by adding another pin to ground it separately, and resulted in the excellent data you see in this lab report. For the first time we testing for our logic gates, we could not get the right output, and that was because the current in our logic circuit could not flows fast enough. We tried to fix that problem by adding hold and delay when testing.

If we were to repeat this lab, we would experiment with using MOSFETs of different dimensions and we would probably use a resistor instead of a diode as the load, as the diode makes analysis far more difficult. One retrospective idea we had afterwards was that we could have made a full adder and all the gates with the diode as the load, and then another full adder and gates with resistors. This way, we could directly compare the performance of the different kinds of loads. Additionally, using one transistor of the same gate dimensions was probably not the best idea, as we would have learned more if we made the another set of the same gates with a different size MOSFET to compare the performance of the circuits based on transistor dimensions. This was a pretty major design flaw that we had, as our entire project was just to see if we could make a working full adder, rather than testing a variety of different configurations and MOSFET characteristics to see how performance changed. We would also start off with double checking our design, to make sure everything was laid out correctly. Not having that transistor grounded on our XOR gate made testing very difficult for us when it came to the Full Adder as we had to use 9 pins to test it, and our capacitor design was fundamentally wrong as it did not show any capacitance at all. Besides, we will leave more standing alone testing structures. More specifically, we will leave diodes load with MOSFETs stage by stage, which will make our life more easier when testing the output low and high and do the load line analysis for the gates. Overall, this lab and class allowed us to understand and become involved in the process required to fabricate the very transistors we do calculations with daily. We became well familiar with the laborious procedure of fabricating such chips and also gained insight as to why the device itself functions the way it does based on its components and the steps taken to put it together. It was a very valuable experience and gave us tools and knowledge that will no doubt be useful in the future.

References:

NMOS Digital Circuits:
https://ftp.utcluj.ro/pub/users/dadarlat/circ_analognumeric-calc/Curs5-engl.pdf

Rabaey, Jan M., Anantha P. Chandrakasan, and Borivoje Nikolić. *Digital Integrated Circuits: A Design Perspective*. Delhi: PHI Learning Private Limited, 2013.

Bayoumi, M.a., G.a. Jullien, and W.c. Miller. "An Area-time Efficient NMOS Adder." *Integration, the VLSI Journal*1, no. 4 (1983): 317-34. doi:10.1016/s0167-9260(83)80005-4.