Final Lab Report: NMOS Transistor

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Abstract:
After a full quarter of practicing the techniques involved in making steady state semiconductor devices including applying photoresist, optical lithography, growing oxides, mask alignment, and familiarizing ourselves with the equipment and tools necessary to perform each part of the process, we were given the task of making our own MOSFET devices. The lab skills that we acquired over the course of the quarter are both applicable and important as semiconductor fabrication is a rapidly advancing area of study in electrical engineering.

For our final project, we started by growing a layer of wet oxide and then applying the first mask to each sample with photoresist. We then etched the oxide away with the HF, removed the photoresist, and deposited our phosphorus to be driven in later. After an HF dip to remove the phosphorus glass that formed on our chips, we grew another layer of oxide while simultaneously driving in our dopants. We applied the second mask on photoresist again and then etched the exposed oxide, forming more features for our device. We grew another layer of dry oxide, further driving in our dopants, and then applied mask 3. Again, we etched the exposed oxide with HF and removed our photoresist, creating the final silicon dioxide features. Our fourth and final mask was applied, this one for the metal deposit and liftoff. We deposited aluminum over the entire area of all our samples, and then removed the photoresist to lift off the aluminum that was deposited over it, which we didn't want as part of our device. This concluded the actual fabrication process of the lab, taking roughly a week as a group of five. However, it wasn't a working MOSFET if it didn't display the characteristics of a one, so we used a very precise testing machine to view the IV curves that our devices created, ensuring that our processes were carried out correctly and the chip was functioning as it was supposed to. The masks that we used also made resistors and capacitors for us to test, providing more ways to tell if our device was fabricated properly.

Test Samples

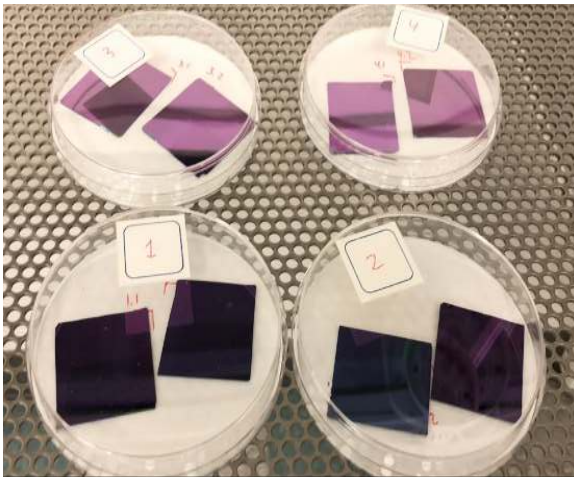


Figure 1

Final Devices Under Microscope

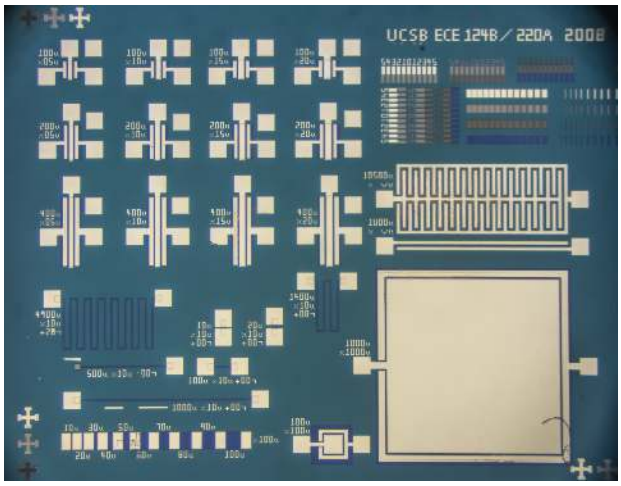


Figure 2

Thankfully all of the components of the chip worked, but it was certainly close, as only 1 out of the 4 chips that we made performed the way it was supposed to. It was truly gratifying to see that our project that we had worked on so tediously performed exactly how it was supposed to, and it was a great learning experience. Sequentially going through the entire procedure of building a semiconductor really helped to form the concepts taught in class into one cohesive idea.

Procedure

Over the last two weeks we worked in the clean room in order to successfully fabricate a properly working MOSFET device. This involved multiple visits to the clean room where we worked with various processes, including oxidation, pre-deposition, drive-in, metal evaporation and lift-off along with multiple different wafer cleaning techniques to ensure the accuracy of a working device.

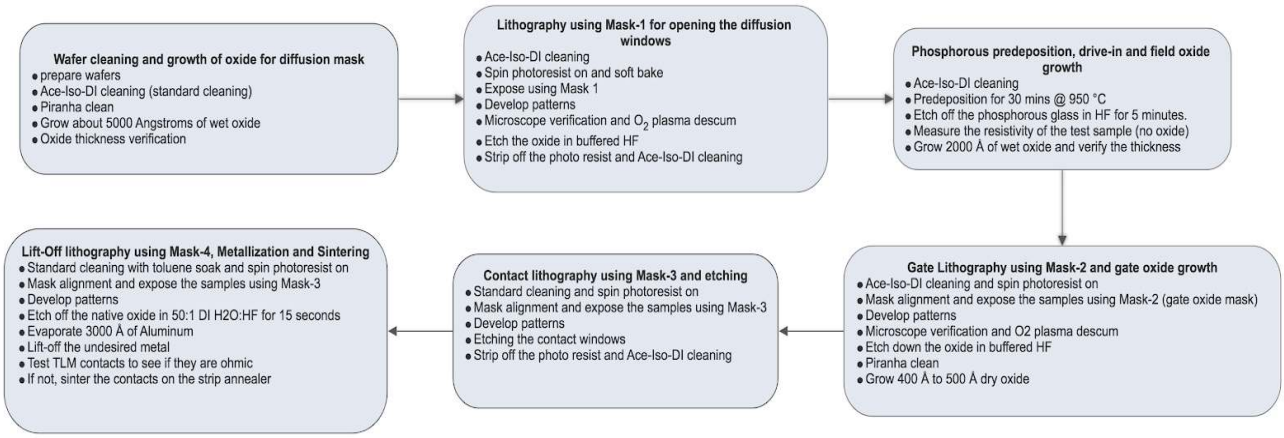


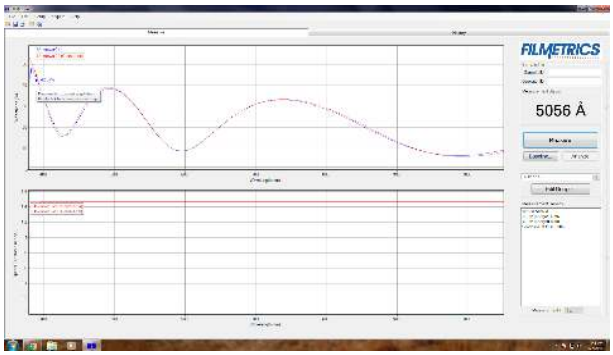
Figure 3

Day 1: Wafer cleaning and growth of oxide for diffusion mask

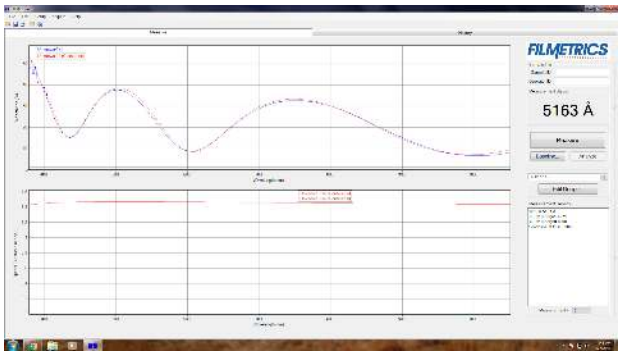
After properly gowning up in clean room attire, we used the diamond tipped scribe to cleave two p-type <100> silicon wafers of 10-30 ohm-cm into 8 individual samples (Figure 1). We, then, cleaned each sample using proper wafer cleaning by immersing them in acetone (ACE) and isopropyl alcohol (ISO) before using the DI water and N_2 gas to dry them. Proceeding wafer clean, we measured the resistivity using the four point probe and got 16.35 ohm-cm, verifying the resistivity measurement that we wanted. Before oxidizing our wafers, we performed a piranha clean using a mixture of hydrogen peroxide (H_2O_2) and sulfuric acid (H_2SO_4) for ten minutes. We, then, cleaned our wafers with HF and DI water in order to remove any small layer of oxide that might have formed due to the peroxide. To operate the furnace, we followed several preparatory procedures, including preheating the furnace, setting the bubbler, and purging the system with N_2 gas. We then replaced the N_2 gas with O_2 gas. Placing our wafers into the furnace was a delicate procedure: first we put them on the sample holder, which was then placed in a boat (quartz elephant) that we pushed into the furnace with a glass rod. We began with a ten minute dry oxidation, followed by an 1 hr 10 minute wet oxidation (which we did by turning off the O_2 and turning on the process switch), and finishing with another ten minute dry oxidation. We took the wafers out of the furnace and after letting our wafers cool we measured the thickness of the SiO_2 layer with an Applied Materials ellipsometer and a Filmetrics thin film analyzer to get an initial layer thickness of 5000-5200 Å (Shown in images below). The

variations in the thicknesses is because of the temperature variation due to the placement of the chip in the furnace.

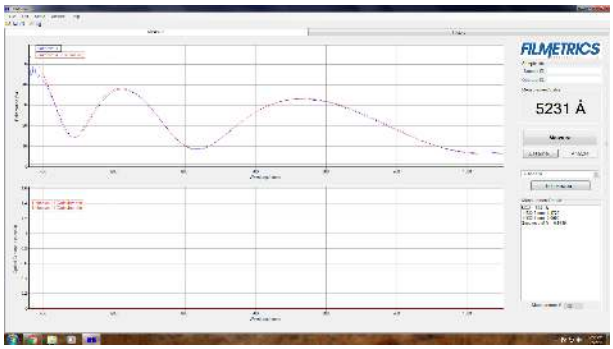
Sample 1.1



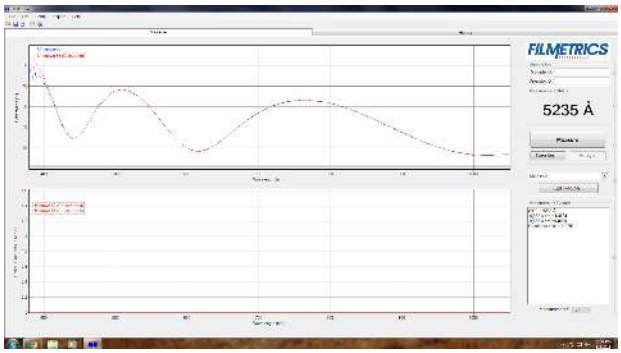
Sample 2.1



Sample 3.2



Sample 4.2



Day 2: Lithography using Mask-1 for opening the diffusion windows

After day 1, we had about 5000 Å of wet SiO_2. We started with standard Ace-Iso-DI cleaning, dehydration baking for 3 minutes, and placing wafers under the HMDS vapor deposition hood for 3 minutes. Then we spun photoresist on and soft baked for 1 minute. Then we used Mask-1 to expose diffusion regions and exposed under UV light for 12 seconds. We developed each chip at a time using 4:1 DI H_2O:AZ 400K developer for 70 seconds for Sample 3.1 and Sample 3.2 and 75 seconds fo all other samples and then examine under the microscope.

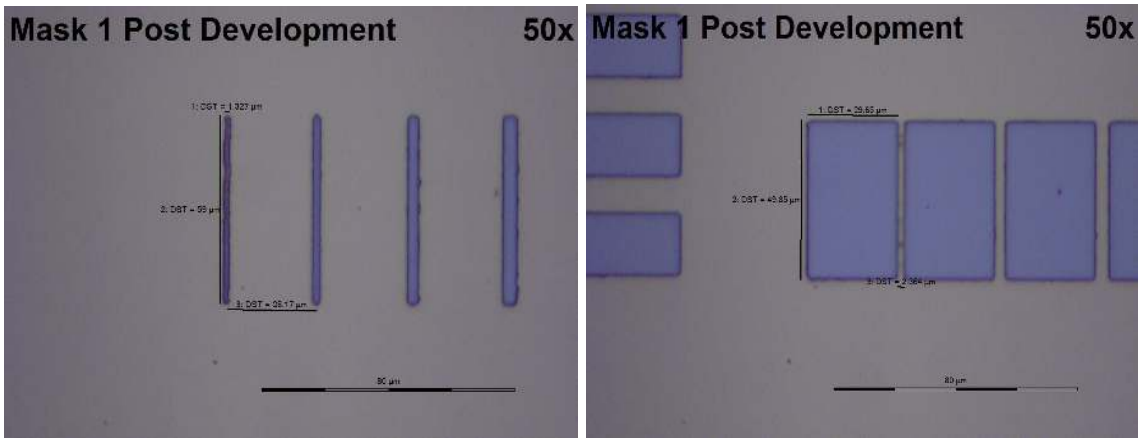


Figure 4 Sample 3.2 Mask 1 Post Development

Before we etch off oxide, we performed O_2 plasma descum. Then we etched one chip to verify the etching rate and calculate how long does it take to etch off all 5000 Å oxide with 20% over-etching. Before etching, we immersed the wafer in DI for 1 minute with agitation before placed it in HF. This prevents bubble formation and ensures uniform etching in HF.

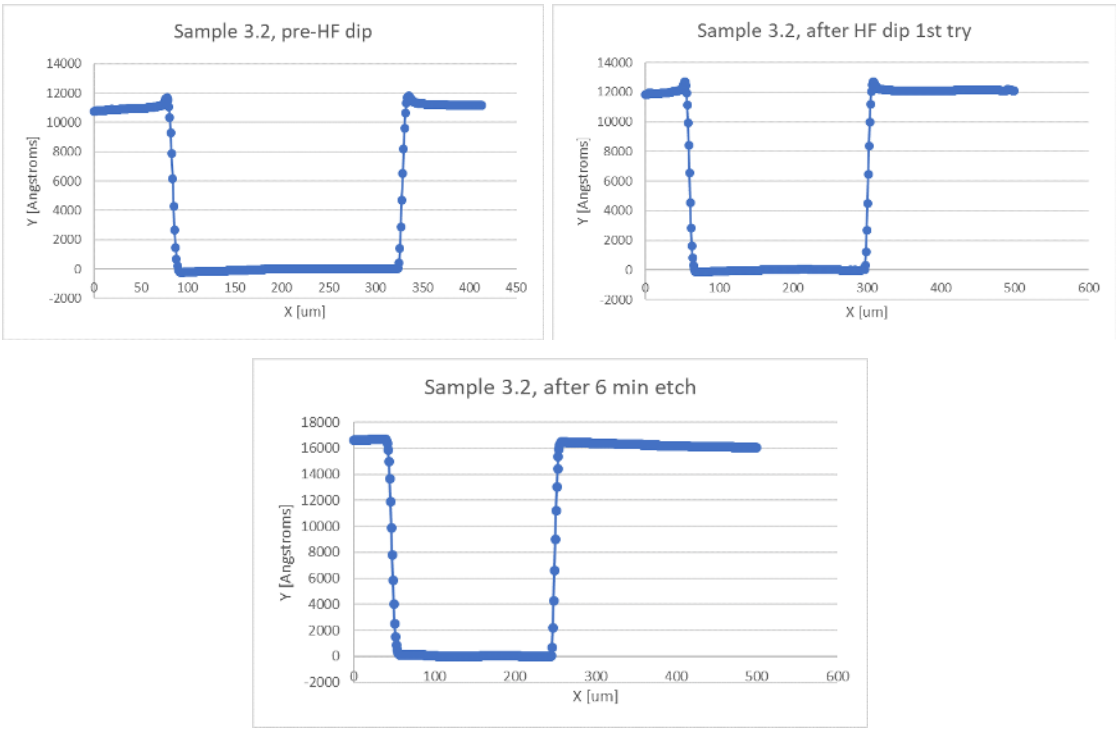


Figure 5 Dektak Measurement Sample 3.2 Pre-Etching, After 1 min Etching, and After 6 mins Eching

As shown in figure 5, we started at a difference of 11,000 and after etching the sample for 1 minute, the different is 12,000. This means we etched off (12000-11000) = 1000 Å SiO_2. For 5000 Å SiO_2 and 20% overetching, which means we should etch off 6000 Å, we etched samples for 6 minutes. The final difference shown by the Dektak machine is about 17,000, this shows that we etched off (17000-11000) = 6000 Å SiO_2.

To verify that we have etched off all SiO_2 in the desired region, we examined them under the microscope to compare the color with that of a pure silicon.

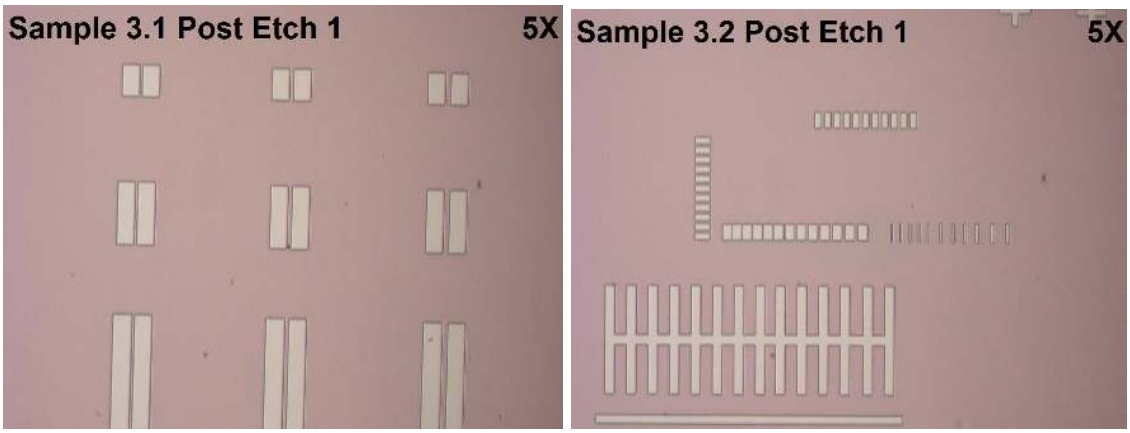


Figure 6 Sample 3.1 and Sample 3.2 After Etching

We, then, removed photoresist by dipping in acetone for 1 minute for initial removal, followed by a minute in acetone in a sonic bath, then another minute in 2-propel in the sonic bath. This is the procedure for every photoresist removal.

Day 3: Phosphorus predeposition, drive-in and field oxide growth

For phosphorus predeposition, we will be using the PDS (planar diffusion source) PH-950 n-type solid sources. Prepare the wafers for the predeposition by going through the standard Ace-Iso-DI cleaning procedure and Piranha Clean, including a test wafer for predeposition. We did 30 mins for pre-deposition at 950 °C (instead of 15 mins pre-deposition time recommended on the NMOS process handout), see figure 7.

Figure 7: Bob Hill loading samples into the phosphorous furnace

After letting samples to cool, we used 50:1 DI H_2O : HF to remove the phosphorous glass layer formed on the surface of the substrate during the diffusion process. We started by dipping the test wafter into 50:1 DI H_2O : HF for 5 minutes and to see if water beads on the surface since silicon surface is hydrophobic and then dipping wafers into 50:1 DI H_2O : HF for 5 minutes and make sure to see water beads. After removing the phosphorus glass layer, rinse in DI H_2O for 2 minutes and blow dry with N_2 gas. The sheet resistance on the test wafer is about 0.002542 Ω-cm.

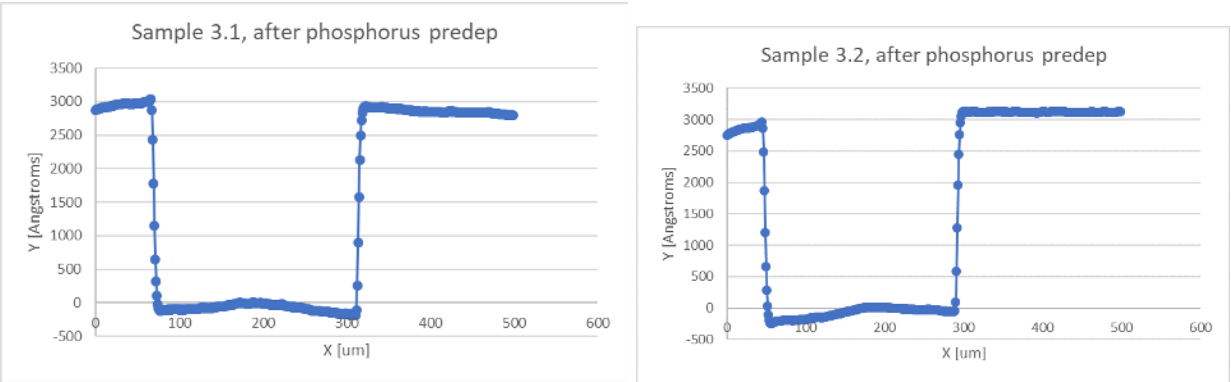


Figure 8 Dektak Results for Sample 3.1 and Sample 3.2 After Phosphorus Predeposition

Then we were ready to grow 2000 Å of wet oxide. Followed by the same procedure as growing 5000 Å oxide before, we had about 6000-6500 Angstroms thick field oxide while the source and drain regions are covered by about 2000 Angstroms of oxide; see figure 8.

Figure 9 Pari Patel loads wafers into the oxide furnace as Bob Hill and Bahar Asghari watch

Day 4: Gate Lithography using Mask-2 and gate oxide growth

We started with standard Ace-Iso-DI cleaning and dehydration bake. Then we placed wafers under the HMDS vapor deposition hood for 3 minutes, spinned photoresist on and soft baked for 1 minute. Then we aligned Mask-2 with Mask-1 and exposed under UV light for 12 seconds. After 70 seconds development in 4:1 DI H_2O:AZ 400K developer, we verified patterns under the microscope.

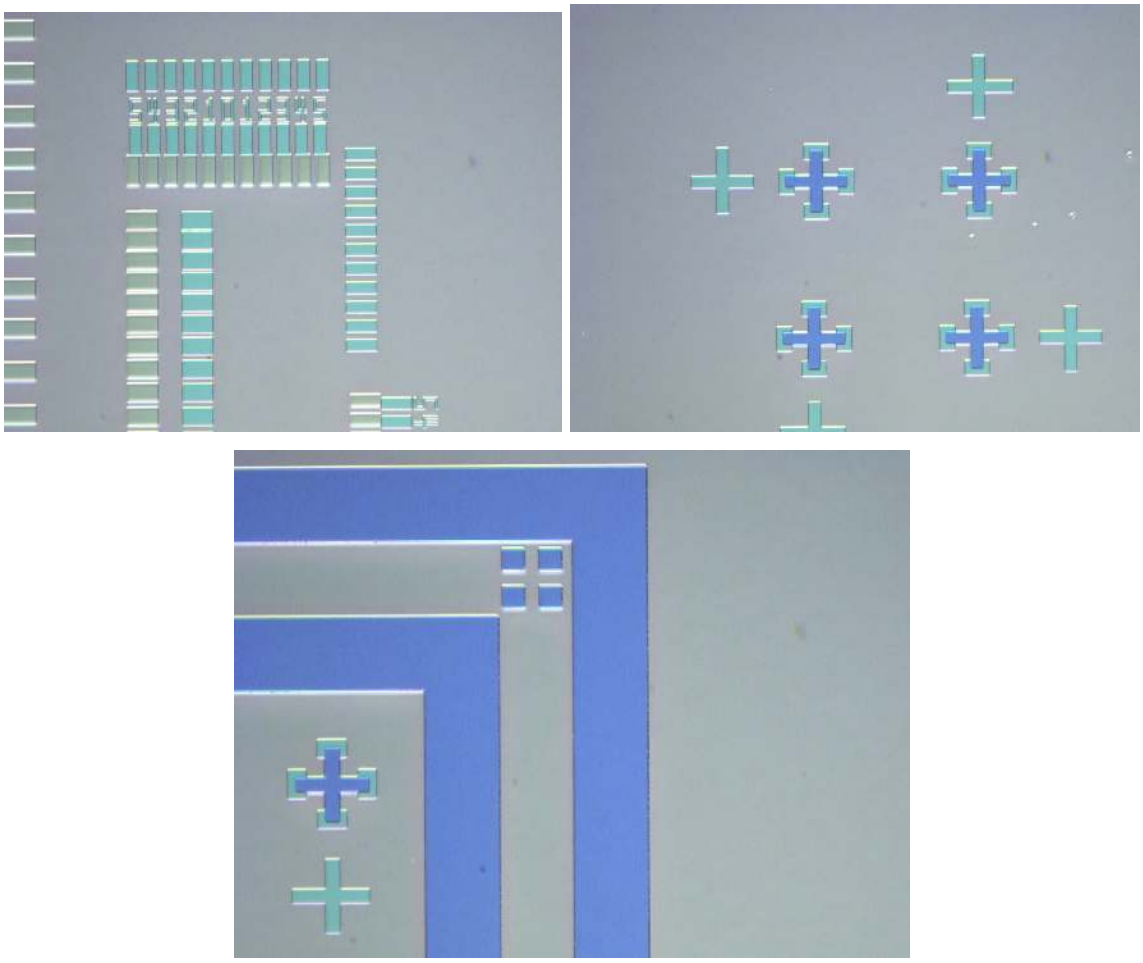


Figure 10 Sample 3.1 After Mask-2 Pattern Transfer

Then we did an O_2 plasma descum and prepared for etching. The etching rate is about 1050 Å/min. After etching the oxide for 6 minutes we stripped the photoresist from the chips and prepared them for oxide growth by piranha cleaning then and a brief HF dip.

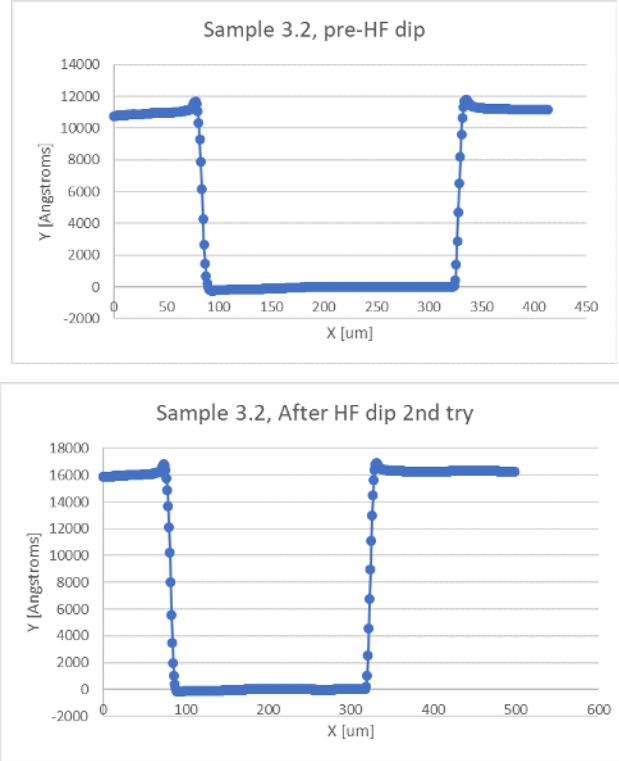


Figure 11: Sample 3.2 before HF dip and oxide growth and after 6 mins etching

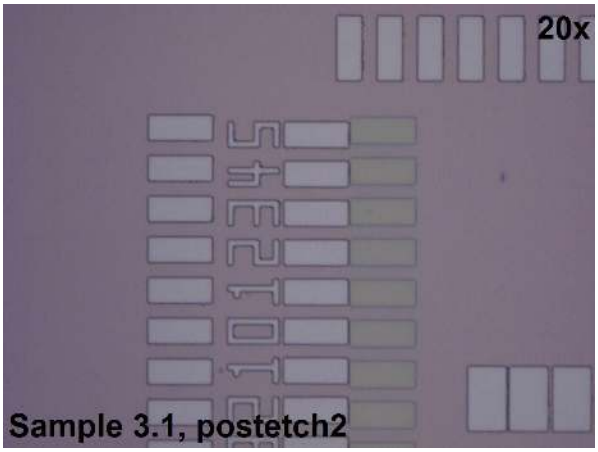


Figure 12: Sample 3.1 after etching

Using the dry oxide growth procedure, we put the wafers into the furnace for 30 minutes. With the Dektak, we confirmed that we had grown about 450 Angstroms of dry oxide on the samples.

Day 5: Contact Lithography and Etching

After having the wafer prepared with the dry oxide of thickness 400 Å to 500 Å, we transferred the pattern from Mask-3 (vias) onto the samples. We used standard lithography techniques to transfer the pattern, starting with a standard Ace-Iso-DI cleaning and dehydration bake, then

placing wafers under the HMDS vapor deposition hood for 3 minutes, spinning photoresist on, and soft baking them each for 1 minute. We aligned Mask-3 with Mask-2 for each chip and exposed them to UV light for 12 seconds. After 115 seconds development in 4:1 DI H_2O:AZ 400K developer, we observed the newly formed patterns under the microscope. After development, the photoresist covered the gates while the drain and source were left uncovered.

Sample 3.2 After Mask-3 Pattern Transfer

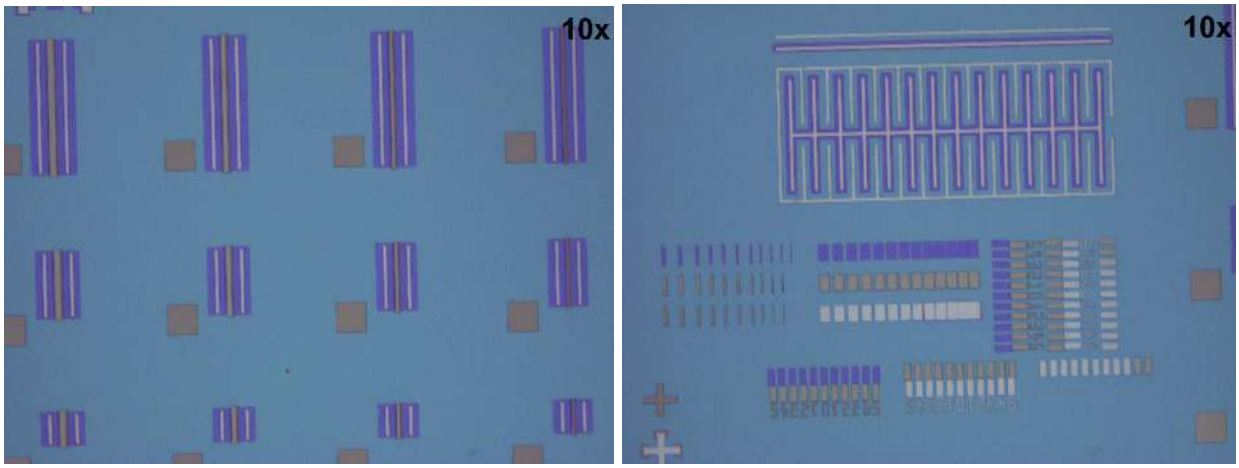


Figure 13

The chips were then placed in HF solution for a 5 minute oxide etch to ensure an overetch of the 450 Angstroms of gate oxide.

After etching away the 450 Angstroms of the gate oxide on all of our samples, it was once again time to remove the old photoresist and prepare it for another layer for Mask-4. This was done with the standard Ace-Iso-DI cleaning and dehydration bake, then placing wafers under the HMDS vapor deposition hood for 3 minutes, spinning photoresist on, and soft baking them each for 1 minute. At this point, the mask alignment process was pretty familiar to us and it didn't take long to apply Mask-4 to our chips. As this final mask was for the metal liftoff step, before we could develop our photoresist we had to dip the samples in a toluene solution for 5 minutes. This is done to harden the outer layer of the photoresist so that when we develop it, it creates a slight lip at the top of the photoresist profile, which is useful as the metal cannot cover the side walls as easily and metal liftoff is significantly neater. However, initially breaking down the strengthened outer layer is a little harder for the developer, so we had to develop our samples for a slightly longer time of 115 seconds, as opposed to the ideal 75. Now with Mask-4 applied and the toluene creating an a nice lip in the photoresist to reduce step coverage, we were ready for the metal deposition and lift-off process.

Day 6: Lift-Off Lithography, Metallization and Sintering

To start this day, we did a quick 50:1 DI H_2O:HF dip before putting the wafers in the metal evaporator. We prepared the evaporator to evaporate 3000 Å of aluminum onto the surface of the wafer and loaded the samples. Pumping down to mid 10^{-6} torr, around 3000 Å of aluminum was deposited. Once the evaporation process was complete, we were ready for the lift-off of the metals to complete our semiconductor. We had ensured the side wall profile of the photoresist was set for a proper lift-off when we had done the toluene dip. To perform the metal lift-off, we placed the wafers in acetone overnight to properly lift-off the PR under the metal. When we came back the next morning, we used a pipette to jet acetone at our chip, agitating the PR to come off along with the undesired aluminum resting on top. We dipped the sample in ISO and DI and blow dried with N_2 after which we were ready to begin testing our devices. You can see where the metal was lifted off in the figure below.

Aluminum Removal

Figure 14

Final Device Under Microscope

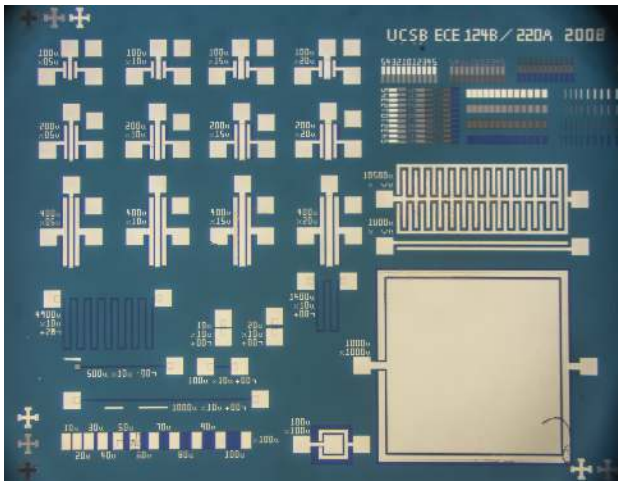


Figure 15

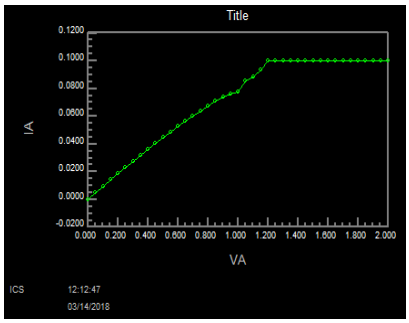
Device Characterizations

To test our devices, we began by TLM contacts in order to see if they were ohmic. For our device, they were ohmic so we did not have to sinter the contacts on the strip annealer. We measured the contact resistance of the ohmic contacts and various I-V curves in order to determine the transconductance, threshold voltage and various other characteristics of the devices that we had fabricated.

Resistance Testing:

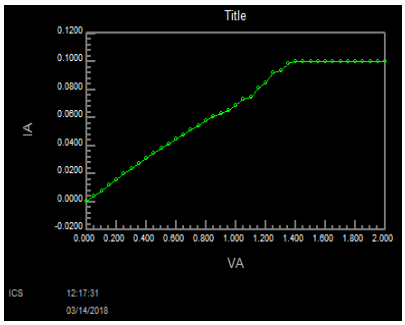
The slope of each IV curve that we measured for the resistors has a slope of 1/R, due to the equation $I = \frac{1}{R}(V)$. In order to measure the resistances of each resistor, we used the inverse slope of the I-V curve.

10 um x 100 um



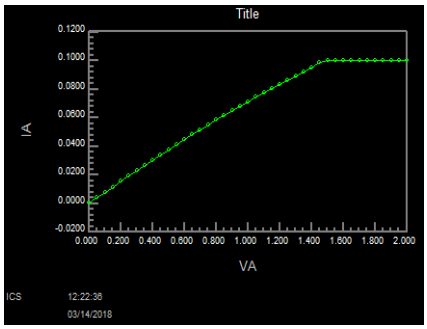
R = 1.2V/0.1A = 12 Ω

20 um x 100 um



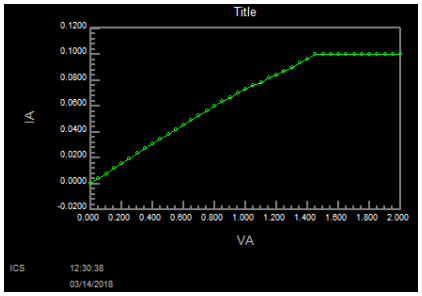
R = 1.375V/0.1A = 13.75 Ω

30 um x 100 um



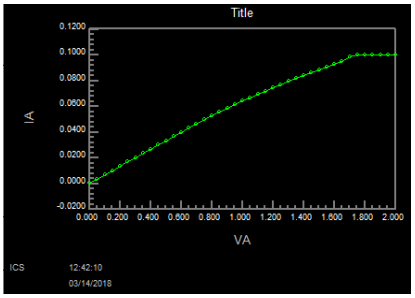
R = 1.45V/0.1A = 14.5 Ω

40 um x 100 um



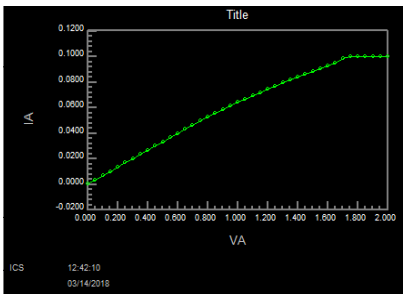
R = 1.45V/0.1A = 14.5 Ω

50 um x 100 um



R = 1.5V/0.1A = 15 Ω

60 um x 100 um



R = 1.75V/0.1A = 17.5 Ω

Figure 16

Resistance vs Length

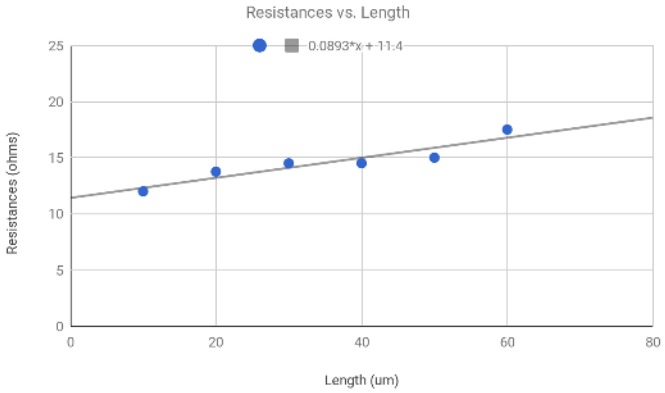


Figure 17

Using the resistance values found from the measured IV curves, we plot a graph of length vs. resistance to see the linear rise in values (as length increases → the resistance increases). The point where the trend line intercepts the y-axis is equal to $2*R_{contact}$. We can see that the value is 11.4 Ω, therefore our contact resistance is equal to 11.4 Ω/2 = 5.7 Ω.

Sheet resistance = (slope of the R vs. L curve) * Width

$$= R_{sheet} = \frac{R}{L}W = 0.0893\,\frac{\Omega}{um} \cdot 100\ um = 8.93\ \Omega/sq$$

From this information, we can see that resistance increases as the length L increases, as equation 1 states. However, our calculated sheet resistance does not plug into the equation to give us the correct resistance that we found, nor does the sheet resistance seem to stay constant. This is most definitely a fabrication problem, and while it might have been better on another chip, when we were taking data, we saw linear curves and assumed that the values were right.

$$R = \frac{\rho}{t}\frac{L}{W} = R_s\frac{L}{W},$$

Equation 1

MOSFETS:

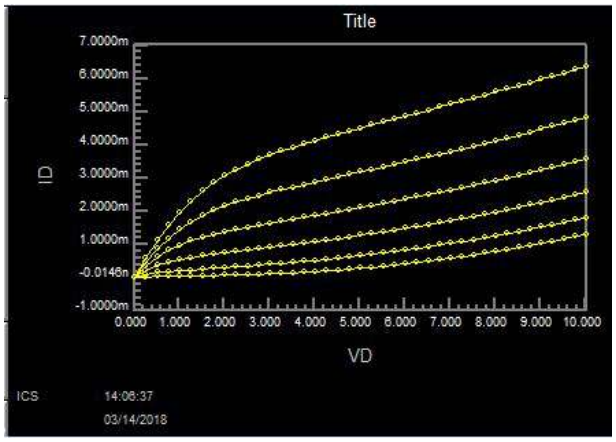
$$C_{ox} \equiv \frac{\varepsilon_{ox}}{t_{ox}}$$ where $\varepsilon ox = 8.85 * 10^{-12} * 3.8$ for SiO2. Using 450 Angstroms as our oxide thickness, we get Cox = 0.07473.

Electron mobility = gd/[(Z/Lg)*Cox*(Vg-Vth)

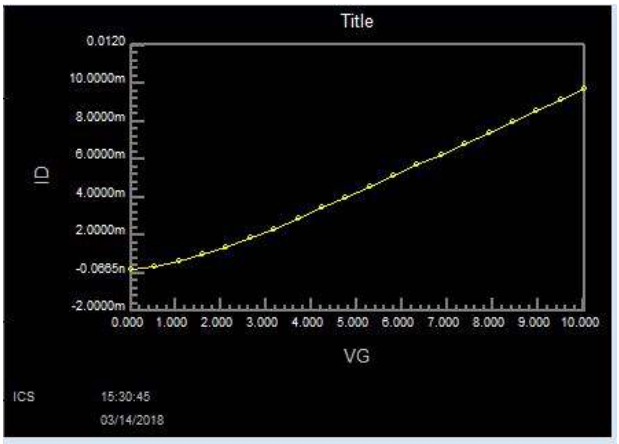
Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

For the following data, we assumed that the threshold voltage occured at I_{DS}=100 uA

<u>100um x 5um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 0.2V

Transconductance gm = slope of Ids vs. Vgs curve=1.053 mS

Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg = 0V, gd = 0 (mosfet is in cut-off)

→ At Vg= 1V, gd = 0.5073 mS

→ At Vg= 2V, gd = 0.6764 mS

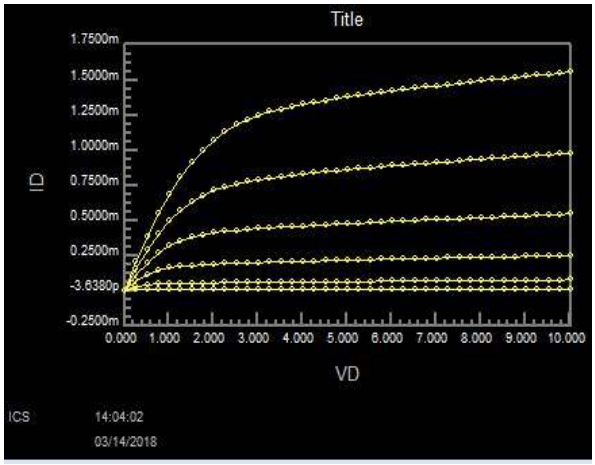
→ At Vg= 3V, gd = 0.7610 mS

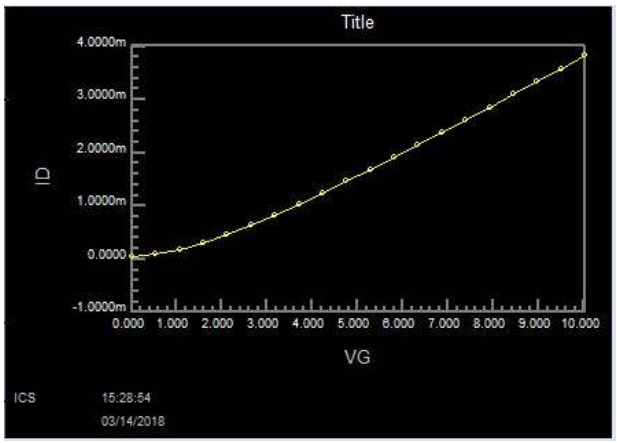
→ At Vg= 4V, gd = 1.439 mS

→ At Vg= 5V, gd = 1.507 mS

→ At Vg= 5V, Gd = (1/5)*4.5 mA = 0.9 mS

100um x 10um





Ids vs. Vds Curve Ids vs. Vgs Curve

Threshold voltage V_{th} = 0.4V

Transconductance gm = slope of Ids vs. Vgs curve= 0.435 mS

Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cut-off)

→ At Vg= 1V, gd = 0.25 mS

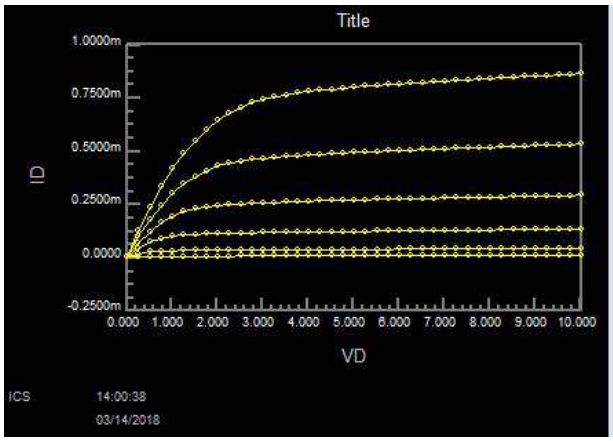
→ At Vg= 2V, gd = 0.355 mS

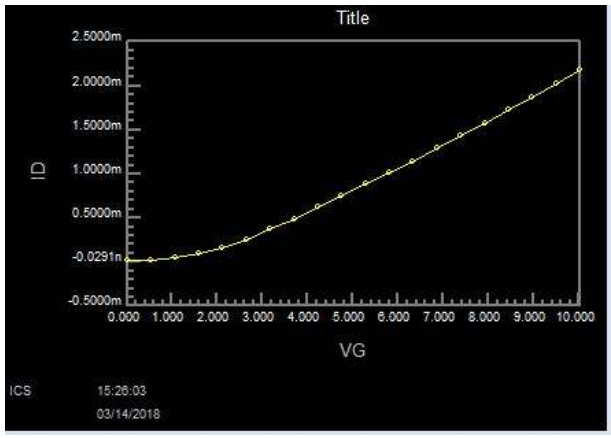
→ At Vg= 3V, gd = 0.375 mS

→ At Vg= 4V, gd = 0.433 mS

→ At Vg= 5V, gd = 0.656 mS

100um x 15um





Ids vs. Vds Curve Ids vs. Vgs Curve

Threshold voltage V_{th} = 0.8V

Transconductance gm = slope of Ids vs. Vgs curve= 0.286 mS

Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cut-off)

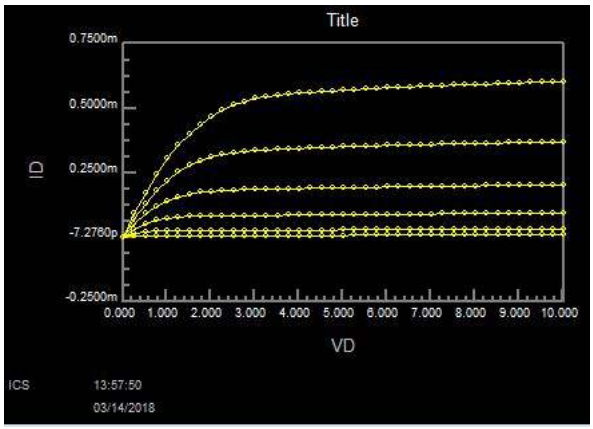
→ At Vg= 1V, gd = 0.125 mS

→ At Vg= 2V, gd = 0.1875 mS
→ At Vg= 3V, gd = 0.209 mS
→ At Vg= 4V, gd = 0.225 mS
→ At Vg= 5V, gd = 0.25 mS

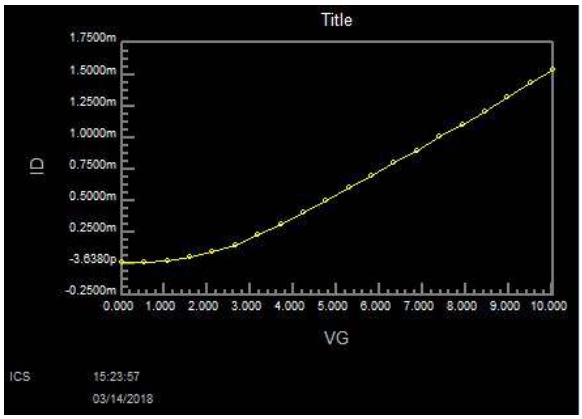
Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

→ At Vg= 5V, Gd = (1/(5))*0.8 mA = 0.16 mS

<u>100um x 20um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 0.9V

Transconductance gm = slope of Ids vs. Vgs curve= 0.208 mS

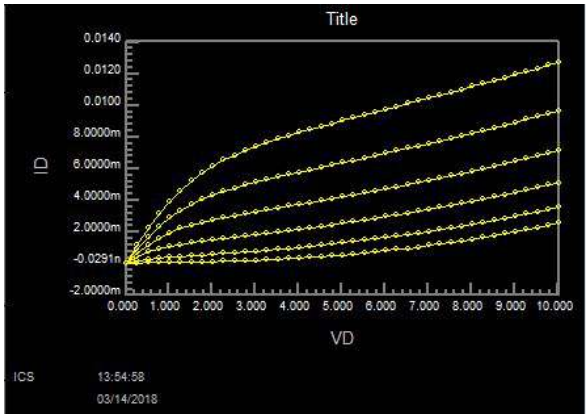
Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cutoff)
→ At Vg= 1V, gd = 0.0125 mS
→ At Vg= 2V, gd = 0.1458 mS
→ At Vg= 3V, gd = 0.015 mS
→ At Vg= 4V, gd = 0.214 mS
→ At Vg= 5V, gd = 0.22 mS

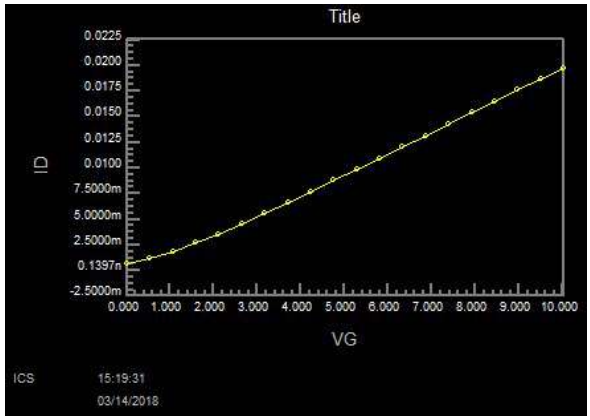
Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

→ At Vg= 5V, Gd = (1/(5))*0.6 mA = 0.12 mS

<u>200um x 5um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = -0.01V

Transconductance gm = slope of Ids vs. Vgs curve= 2.083 mS

Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cutoff)

→ At Vg= 1V, gd = 0.53 mS

→ At Vg= 2V, gd = 0.75 mS

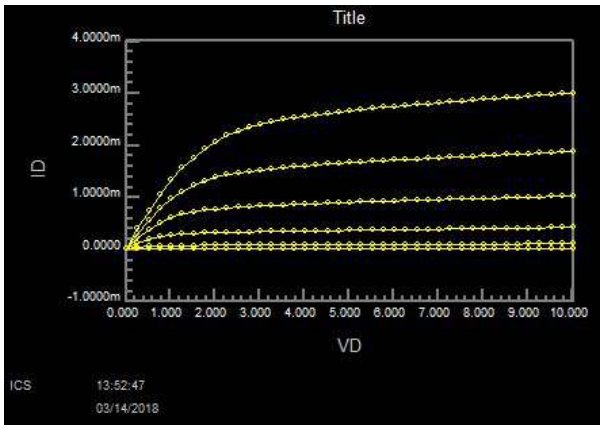
→ At Vg= 3V, gd = 1.25 mS

→ At Vg= 4V, gd = 2.8 mS

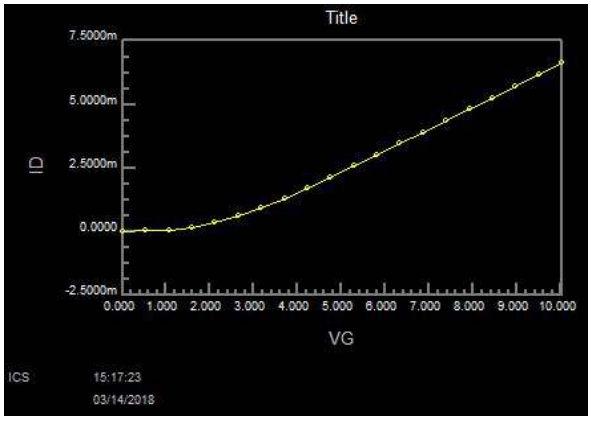
→ At Vg= 5V, gd = 4 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

<u>200um x 10um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 1.5V

Transconductance gm = slope of Ids vs. Vgs curve= 0.806 mS

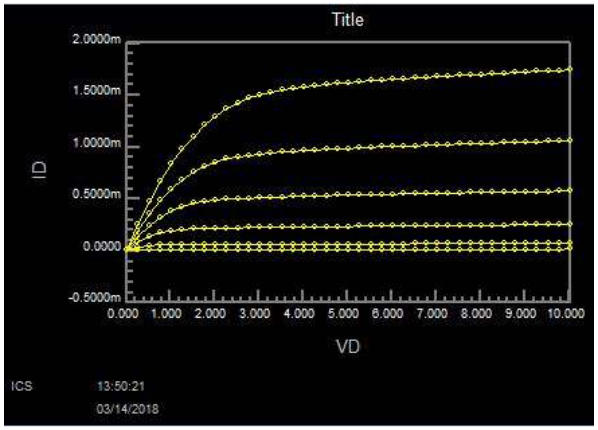
Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cutoff)

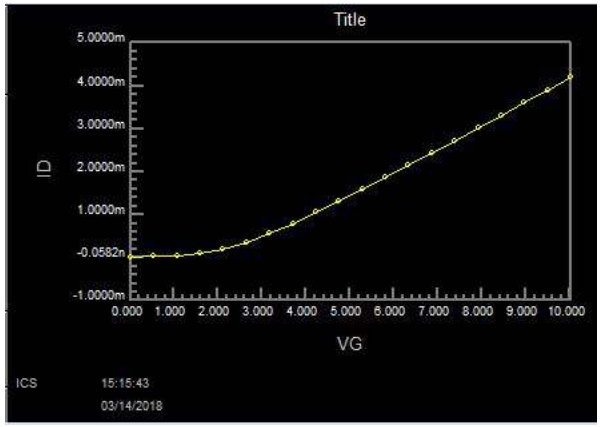
→ At Vg= 1V, gd = 0.12 mS
→ At Vg= 2V, gd = 0.342 mS
→ At Vg= 3V, gd = 0.611 mS
→ At Vg= 4V, gd = 0.912 mS
→ At Vg= 5V, gd = 1.39 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

<u>200um x 15um</u>



Ids vs. Vds Curve

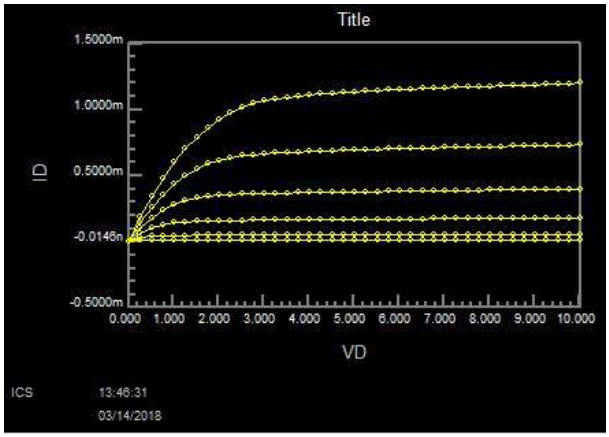


Ids vs. Vgs Curve

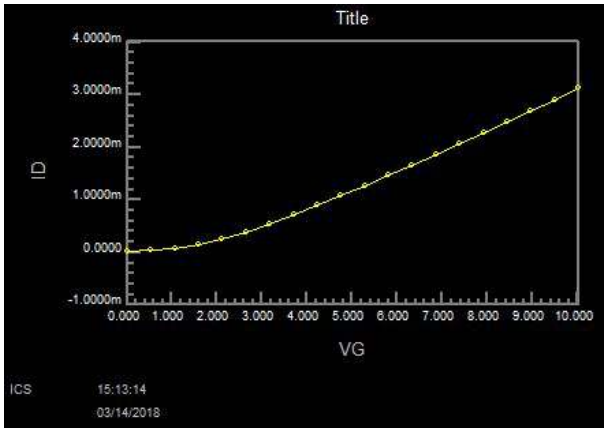
Threshold voltage V_{th} = 1.8V
Transconductance gm = slope of Ids vs. Vgs curve= 0.556 mS
Channel Conductance gd = slope of Ids vs. Vds curve
→ At Vg= 0V, gd = 0 (mosfet is in cutoff)
→ At Vg= 1V, gd = 0.071 mS
→ At Vg= 2V, gd = 0.257 mS
→ At Vg= 3V, gd = 0.377 mS
→ At Vg= 4V, gd = 0.625 mS
→ At Vg= 5V, gd = 0.75 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

<u>200um x 20um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 1.9V

Transconductance gm = slope of Ids vs. Vgs curve= 0.435 mS

Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cutoff)

→ At Vg= 1V, gd = 0.021 mS

→ At Vg= 2V, gd = 0.24 mS

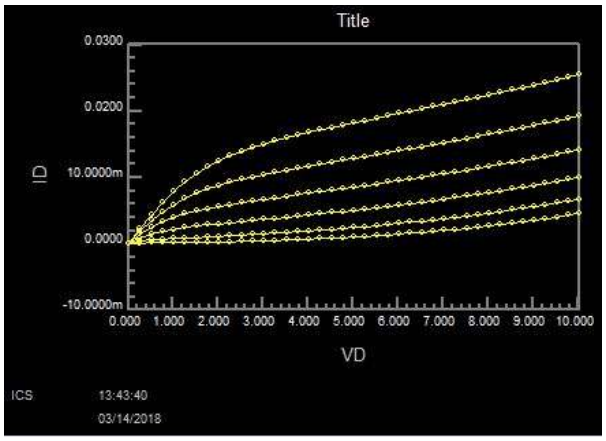
→ At Vg= 3V, gd = 0.275 mS

→ At Vg= 4V, gd = 0.435 mS

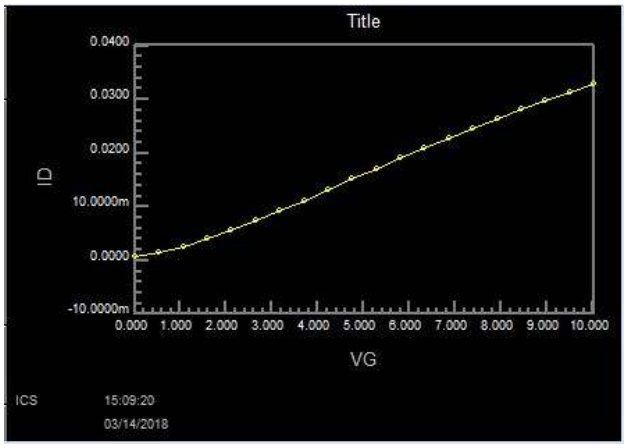
→ At Vg= 5V, gd = 0.667 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

<u>400um x 5um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 0.2V

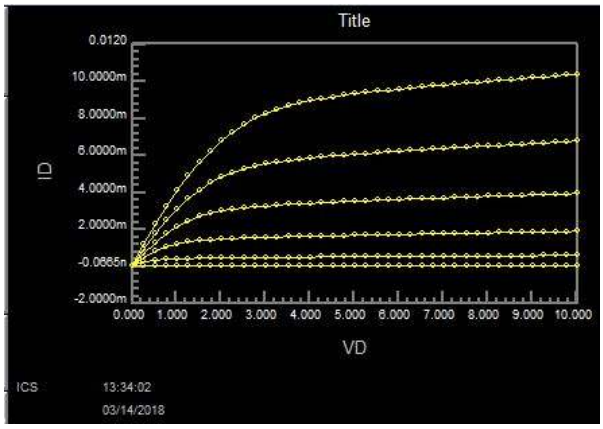
Transconductance gm = slope of Ids vs. Vgs curve= 4.348 mS

Channel Conductance gd = slope of Ids vs. Vds curve

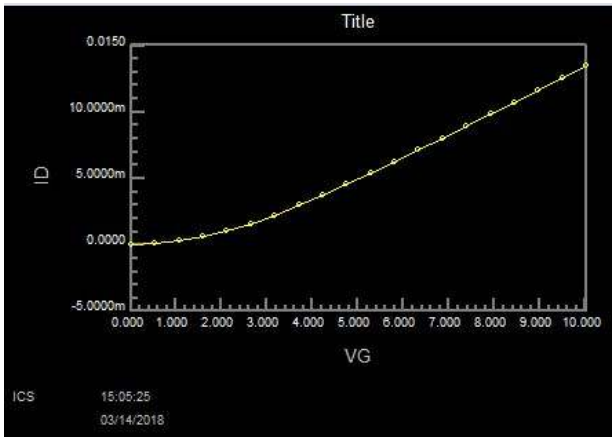
→ At Vg= 0V, gd = 0 (mosfet is in cutoff)
→ At Vg= 1V, gd = 0.366 mS
→ At Vg= 2V, gd = 1.198 mS
→ At Vg= 3V, gd = 2.674 mS
→ At Vg= 4V, gd = 4.464 mS
→ At Vg= 5V, gd = 6.423 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

<u>400um x 10um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 0.8V

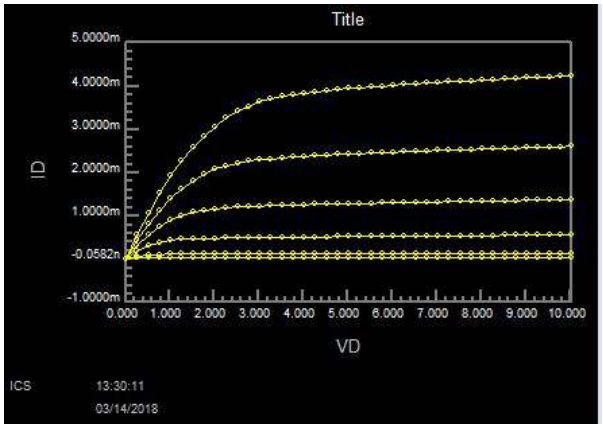
Transconductance gm = slope of Ids vs. Vgs curve= 1.724 mS

Channel Conductance gd = slope of Ids vs. Vds curve

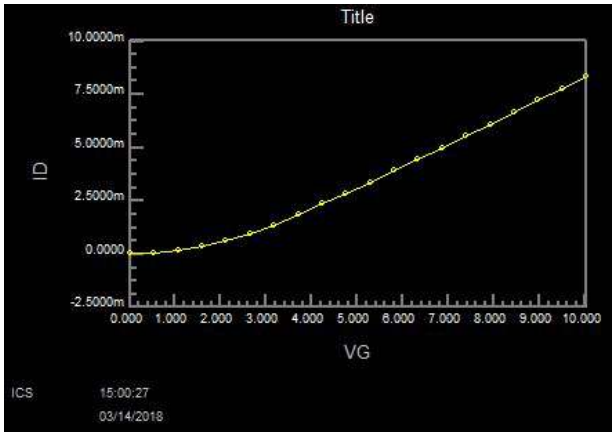
→ At Vg= 0V, gd = 0 (mosfet is in cutoff)
→ At Vg= 1V, gd = 0.101 mS
→ At Vg= 2V, gd = 0.684 mS
→ At Vg= 3V, gd = 1.574 mS
→ At Vg= 4V, gd = 2.524 mS
→ At Vg= 5V, gd = 3.506 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

<u>400 um x 15 um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 1.2V

Transconductance gm = slope of Ids vs. Vgs curve= 1.042 mS

Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cutoff)

→ At Vg= 1V, gd = 0.015 mS

→ At Vg= 2V, gd = 0.177 mS

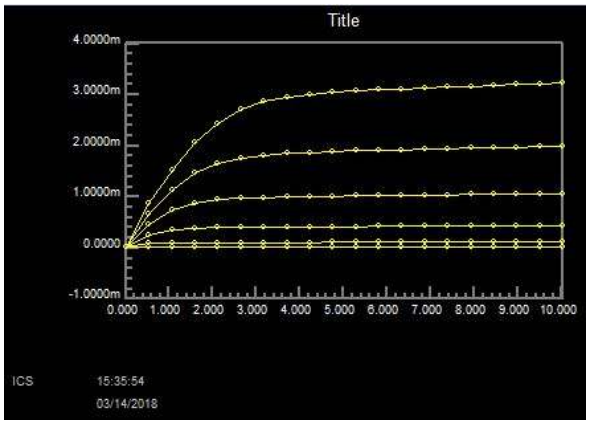
→ At Vg= 3V, gd = 0.592 mS

→ At Vg= 4V, gd = 1.082 mS

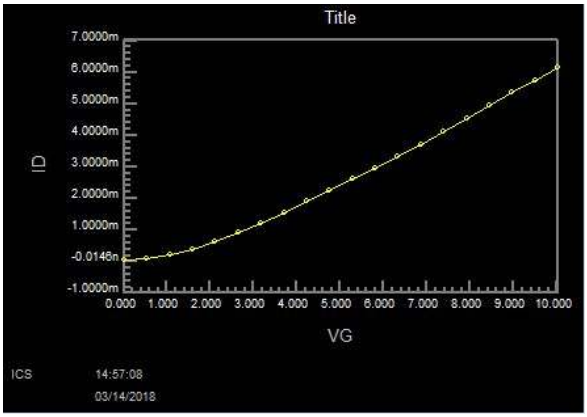
→ At Vg= 5V, gd = 1.586 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

<u>400um x 20um</u>



Ids vs. Vds Curve



Ids vs. Vgs Curve

Threshold voltage V_{th} = 1.4V

Transconductance gm = slope of Ids vs. Vgs curve= 0.714 mS

Channel Conductance gd = slope of Ids vs. Vds curve

→ At Vg= 0V, gd = 0 (mosfet is in cutoff)

→ At Vg= 1V, gd = 0.021 mS
→ At Vg= 2V, gd = 0.187 mS
→ At Vg= 3V, gd = 0.527 mS
→ At Vg= 4V, gd = 0.897 mS
→ At Vg= 5V, gd = 1.274 mS

Output conductance Gd = $\lambda \cdot I_{DS}$, $\lambda = 1/(\textit{early voltage})$, as the early voltage is the x-intercept of Vd vs. Id curve

These IV curves show many of the expected performance parameters of a physical MOSFET device. One major difference, is that we see a negative threshold voltage in many of these devices. We observed that are devices are short channel devices because transconductance is proportional to W/L As the gate width increases, our transconductance goes up, while it decreases when gate length increases, as expected.

As we can see from the results above, the transconductance (gm) is calculated using the slope of the Ids vs. Vgs curve. After calculating each gm, we can see that the value increases as gate width is increased and decreases as gate length is increased.

This aligns with the equation given by:

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)$$

Equation 2

Capacitances:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

Equation 3

where ε_0= 8.854 pF/m, ε_r= 3.9 for SiO_2, A = area of capacitor, and d= thickness of oxide layer

For 100 µm x 100 µm capacitor

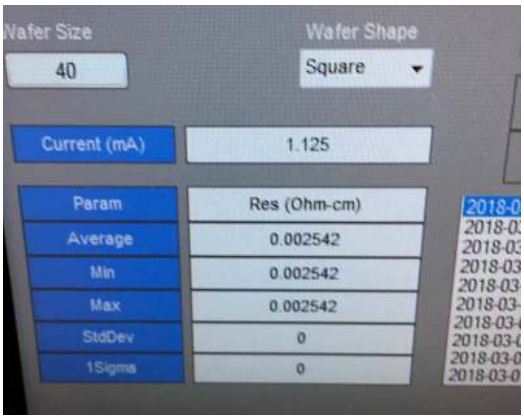
$$C = \frac{8.854 \cdot 10^{-12} F/m * 3.9 * (100 \cdot 10^{-6} m)^2}{450 * 10^{-10} m} = 7.673\ pF$$

Measured capacitance is 35.25 pF
Percent error is 359%. This is likely due to uncertainties in the size of the small capacitor. Percent error is large but true error is only 27pF, which is extremely small. According to our measured capacitance, our oxide thickness in our 100x100 capacitor is only 98 angstroms (assuming the problem is strictly due to oxide thickness), but the error in the measurement is more likely due to other problems in our fabrication process, not the thickness of the oxide.

For 1000 μm x 1000 μm capacitor

$$C = \frac{8.854 \cdot 10^{-12} F/m * 3.9 * (1000 \cdot 10^{-6} m)^2}{450 * 10^{-10} m} = 767.3\ pF$$

Measured capacitance is 714.7 pF
Percent error is 6.86%
Our measured capacitance is much closer to the expected capacitance for our 1000x1000 capacitor. We think that this is probably due to the large size of the feature, which makes the fabrication of the feature much easier. It doesn't rely so much on the accuracy of production. According to our measured capacitance, the thickness of the oxide in this larger capacitor is 449.8 angstroms, which is pretty much exactly what we measured the oxide thickness to be in this feature.



Resistivity of test sample taken after Predeposition

Final Steps

Using the lithography procedure with a fourth mask, we laid the groundwork for the metal (Aluminum) ohmic contacts. Then with metal-lift off, the metal outside of the mask boundaries was removed and only the ohmic contact regions were left with aluminum deposited on top. At this stage our device was ready for testing of the I-V characteristics of the device resistors, capacitors, and transistors. In the end, only one chip remained fully functional and produced ideal output curves. From these curves we observed that devices with larger dimensions produced more favorable output.

Conclusion

This lab was centered around using the skills and techniques we perfected over the course of the quarter to build and test our own MOSFET device from scratch. This process involved knowledge of many procedures, such as photolithography, mask alignment, dry and wet oxide growth, etching, plasma descum, Dektak oxide growth measurement, cleaning with piranha solution, metallization, and metal lift-off. With all of these tools in our arsenal, we were able to grow, layer, and etch oxide in patterns according to three masks to create a silicon wafer with defined channel, source, and drain oxide.

We originally started off with eight chips, but after realizing we could not finish fabricating all eight chips in a timely manner we decreased the number to four chips. Executing the project itself was nearly seamless, with problems easily erased by repeating a cleaning step or adding time to an etch to achieve desired results. By constantly checking our work with the Dektak and other tools, we were able to quickly catch and mitigate problems. While we did experiment with development and pre-deposition times, our results appeared to be consistent. One task that posed some problems was mask alignment and exposure. One chip was lost to this process as during mask 3 it was over exposed. Overall it was difficult to align the chips perfectly but our accuracy was pretty high disregarding the overexposed chip. Another problem that occurred during the lab was that we neglected to perform a plasma descum before we applied mask 3. Because of this, leftover dirt on our wafers caused poorly-defined mask boundaries, and inaccuracies in I-V testing. Another issue occured when we measured our devices and the curves were inverted, making us all nervous that our devices were behaving erratically. Fortunately, this error was caused by a wiring issue and, when resolved, resulted in the excellent data you see in this lab report. If we were to repeat this lab, we would be sure to follow all instructions and not miss any steps to achieve the most accurate results. We would also start off with fewer chips, as eight was far too many and caused fabrication and testing of the chips to take much longer than it should have, given the traffic in lab and long procedure times. Overall, this lab and class allowed us to understand and become involved in the process required to fabricate the very transistors we do

calculations with daily. We became well familiar with the laborious procedure of fabricating such chips and also gained insight as to why the device itself functions the way it does based on its components and the steps taken to put it together. It was a very valuable experience and gave us tools and knowledge that will no doubt be useful in the future.